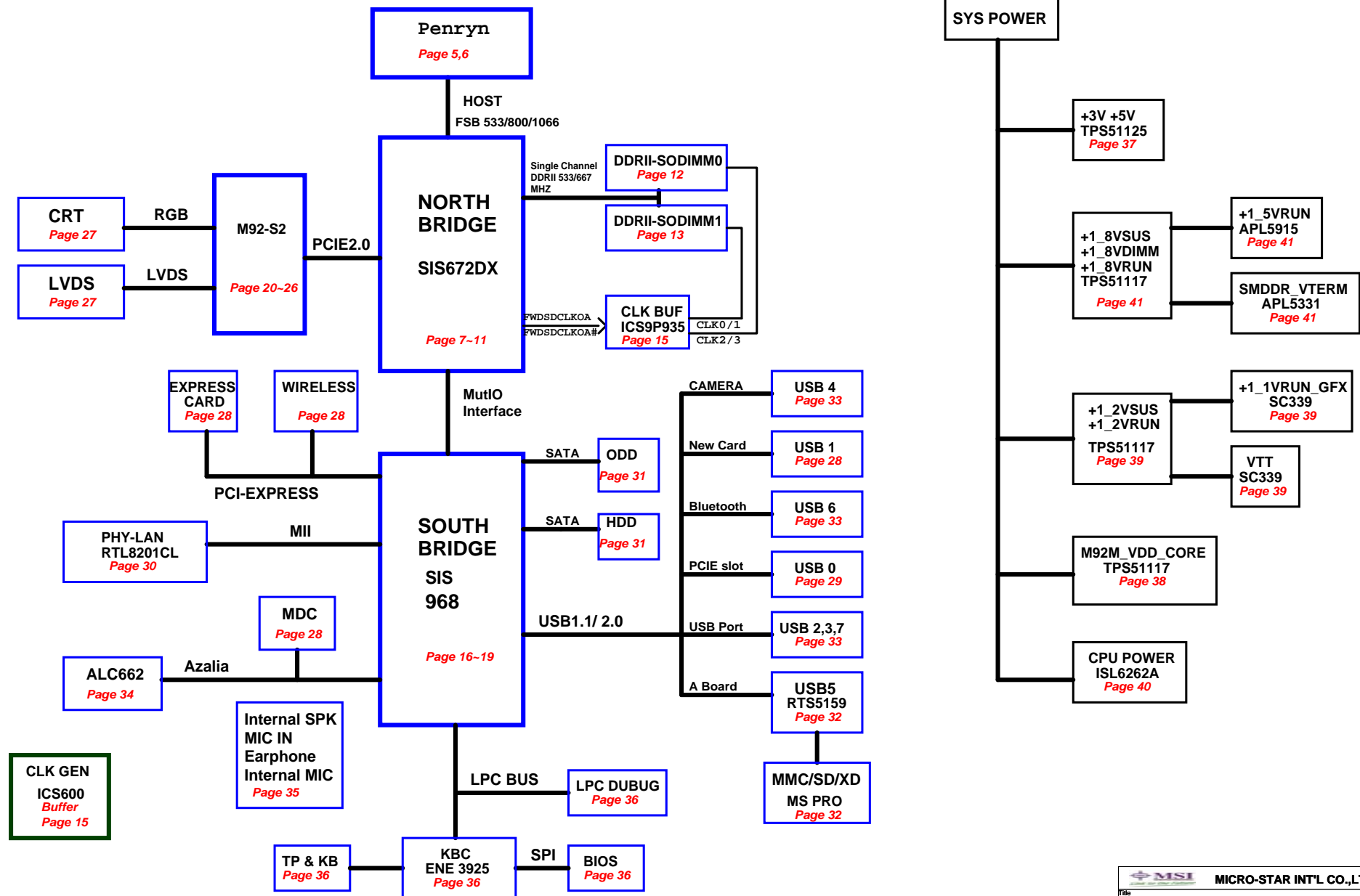
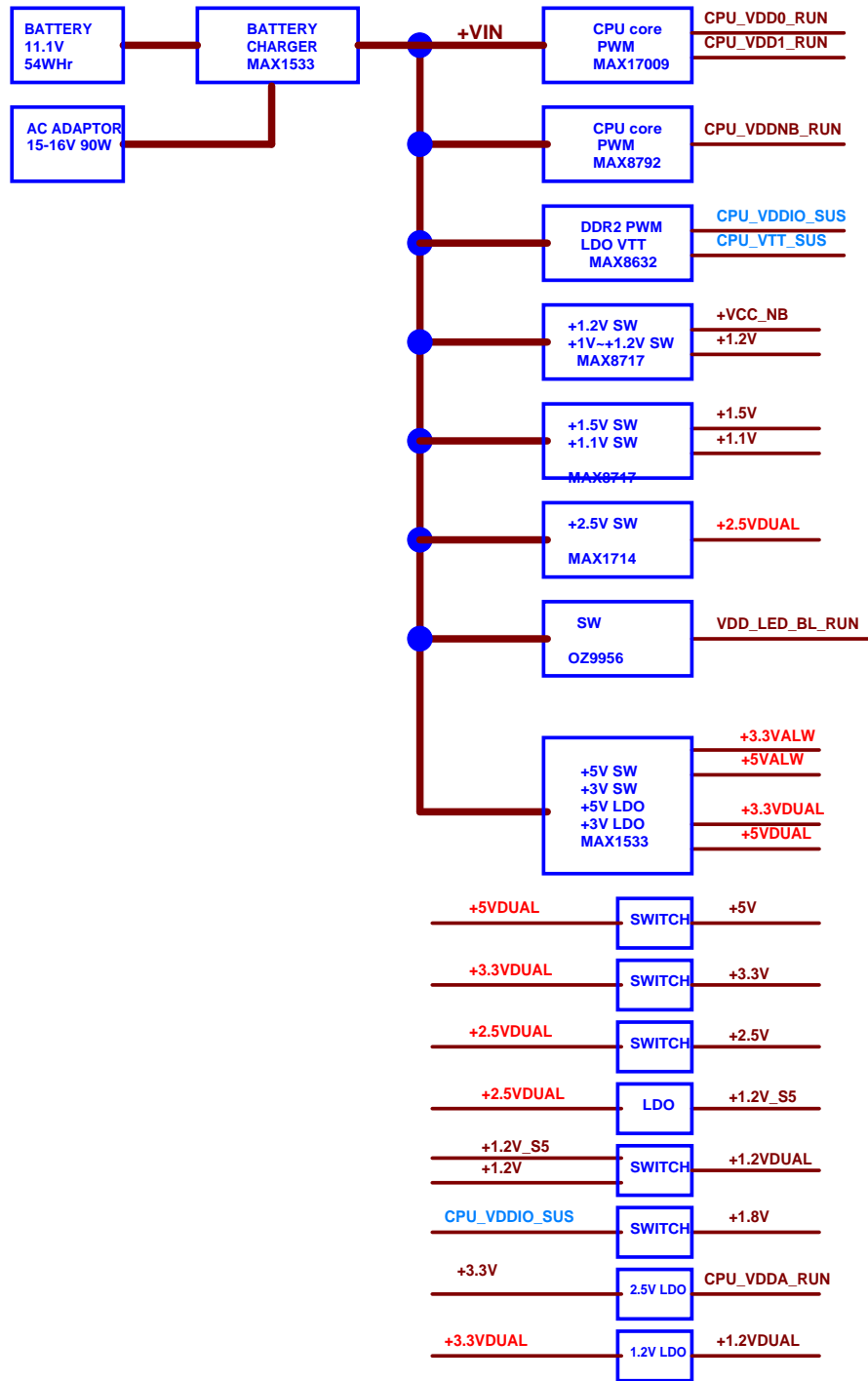


MS-1452 VER : 1.0





AMD S1G2	
CPU_VDDA_RUN	VCCA 2.5V
CPU_VDD0_RUN	VDD0 CORE 0.375-1.500V 18A
CPU_VDD1_RUN	VDD1 CORE 1.375-1.500V 18A
CPU_VDDNB_RUN	VDDNB CORE 1.375-1.500V
+1.2V	TPDA VLD1 1.2V TPDA
CPU_VDDIO_SUS	VDD MEM TPDA
CPU_VTT_SUS	VTT_MEM TPDA

DDRII SODIMM2--SYSTEM	
CPU_VDDIO_SUS	VDD MEM 4A
CPU_VTT_SUS	VTT_MEM 0.5A
DDRII SIDE PORT MEMORY	
+1.8V	BEAD VDD MEM
CLOCK GEN	
+1.2V	BEAD 1.2V 0.2A
+3.3V	BEAD 3.3V 0.5A
HD CODEC	
+3.3V	BEAD 3.3V CORE 0.3A
+5V	BEAD 5V ANALOG 0.1A
AUDIO OP	

RS780	
+1.2V	BEAD VDDHTTX 1.2V 0.5A
+1.1V	BEAD VDDHTRX 1.1V 0.45A
NB_VDD_MUX	BEAD VDDHT 1.1V 0.6A
NB_VDD_MUX	BEAD VDDPCIE 1.1V 0.7A
+1.8V	BEAD VDDA18 1.8V 0.25A
+VCC_NB	BEAD VDDC 1.0V-1.1V 7A
+3.3V	BEAD VDDG33 3.3V 0.03A
+1.8V	BEAD VDDG18 1.8V 0.005A
+1.8V	BEAD VDD18_MEM 1.8V 0.005A
+1.8V	BEAD VDD_MEM 1.8V 0.15A
+3.3V	BEAD AVDD 3.3V 0.135A
+1.8V	BEAD VDDL18 0.08A
+3.3V	BEAD VDDL33 0.22A
+1.8V	BEAD PLLs 1.8V 0.1A
NB_VDD_MUX	BEAD PLLs 1.1/1.2V 0.15A

GBIT ENTHENET	
+1.2VDUAL	BEAD 1.2V 0.5A
+2.5VDUAL	BEAD 2.5V 0.5A
+3.3VDUAL	BEAD 3.3V 0.5A

SMSC1100--EC	
+3.3VDUAL	Jumper 3.3V 0.5A
+3.3VALW	RS740/RS780

LCD PANEL	
+3.3V	SW 3.3V 1.5A
+5V	BEAD 5V 0.5A

BACK LIGHT	
+5V	+5V
VDD_LED_BL_RUN	LED_BL
+VIN	+VDD_MAIN

USB X2 FR	
+5VDUAL	5VDual
USB X7 FR	
+5VDUAL	5VDual

EXPRESS CARD	
+1.5V	1.5V (S0, S1) 0.7A
+3.3V	3.3V (S0, S1) 1.3A
+3.3VDUAL	3.3V (S3, S5) 0.3A

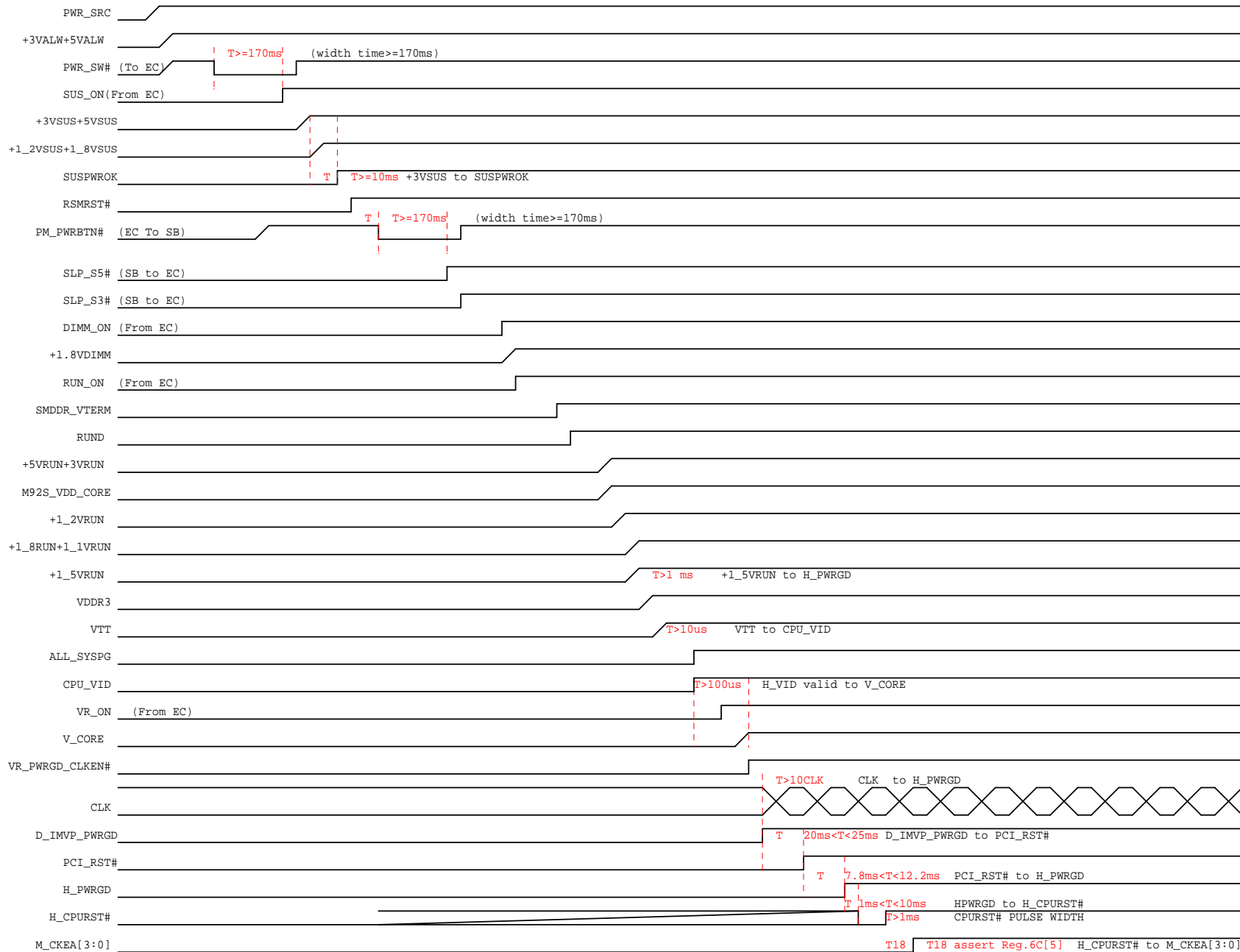
MINI PCIE SLOT1	
+1.5V	1.5V (S0, S1) 0.7A
+3.3V	3.3V (S0, S1) 1.3A
+3.3VDUAL	3.3V (S3, S5) 0.3A
SIM	

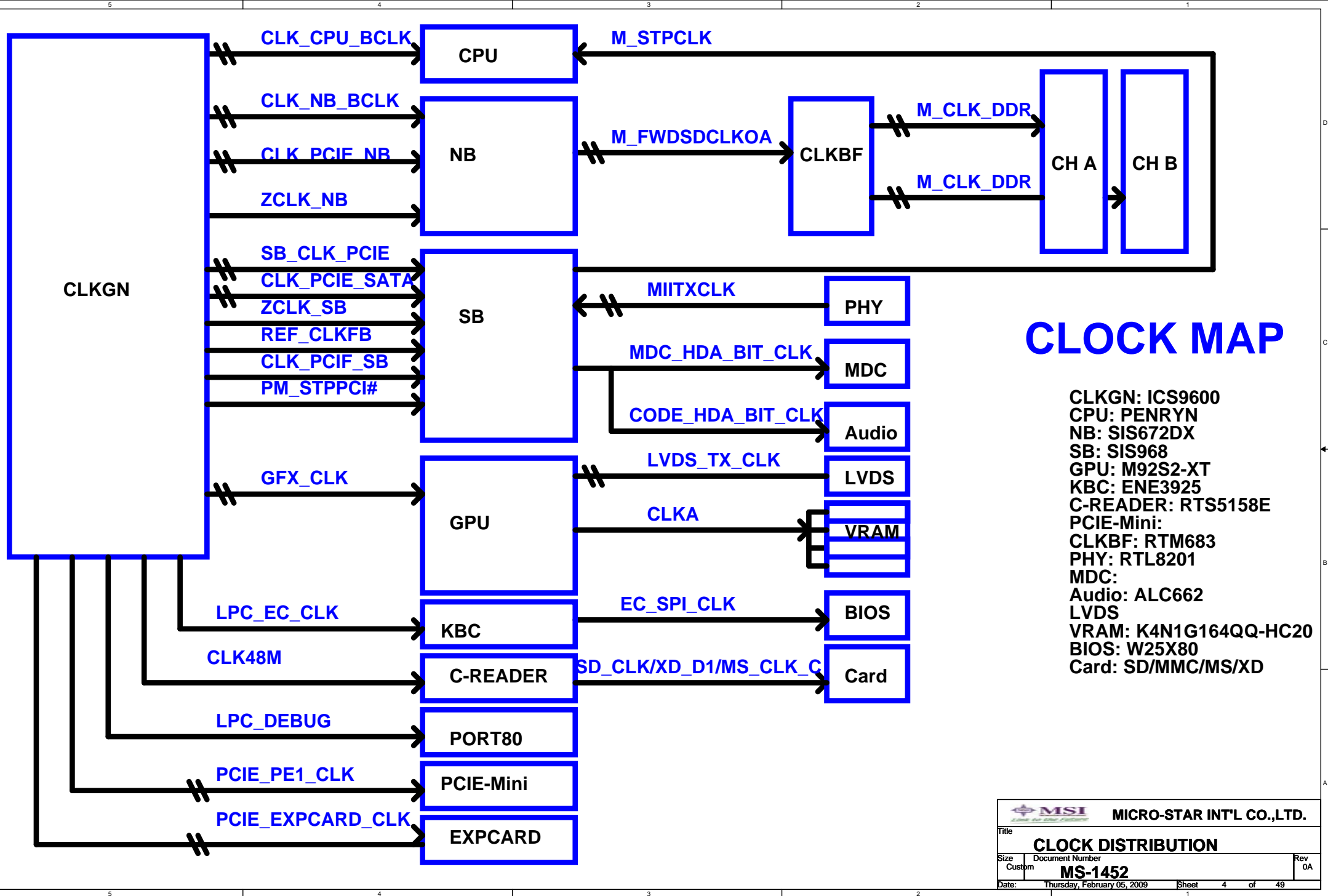
MINI PCIE SLOT2	
+1.5V	1.5V (S0, S1) 0.7A
+3.3V	3.3V (S0, S1) 1.3A
+3.3VDUAL	3.3V (S3, S5) 0.3A

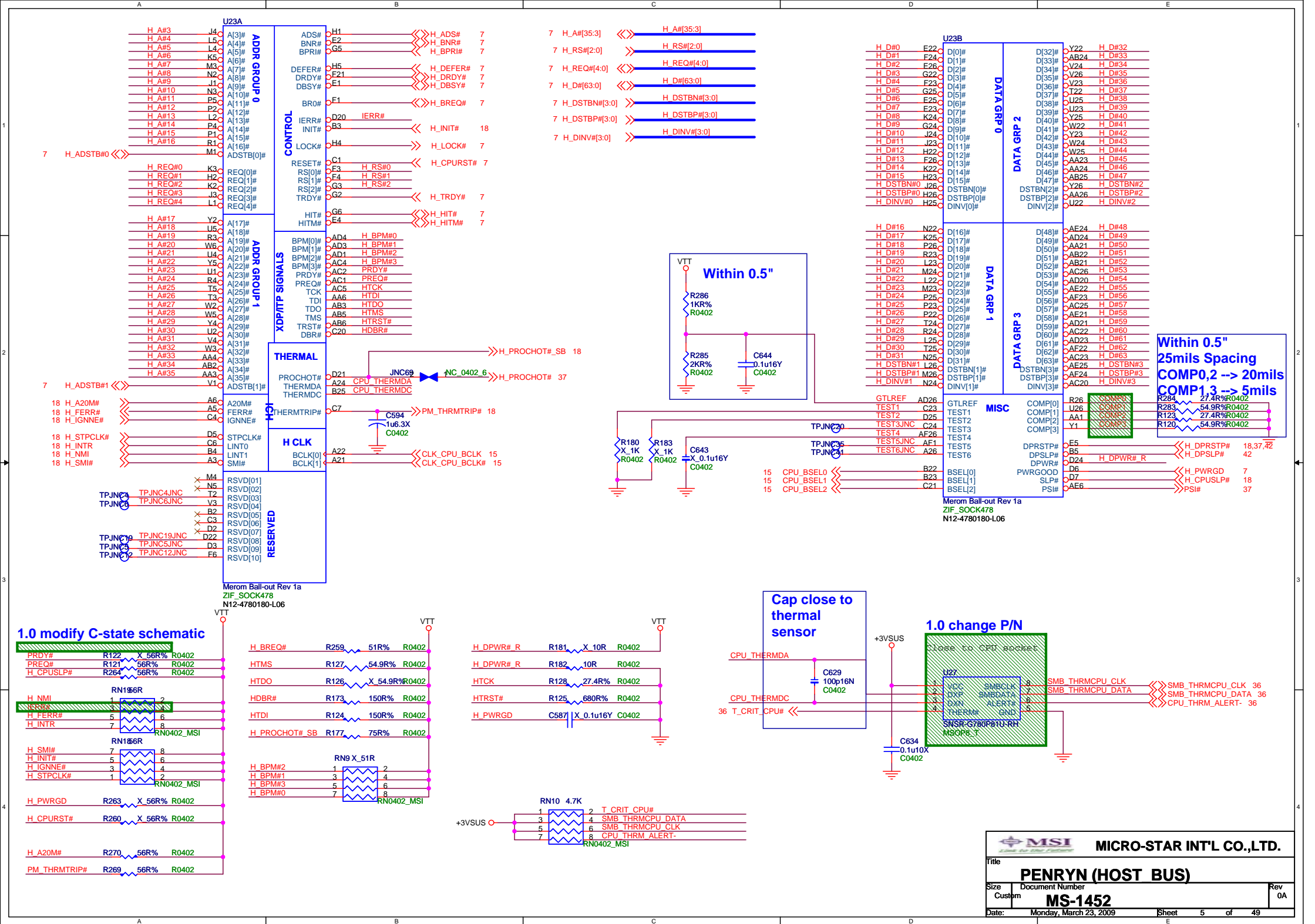
MINI PCIE SLOT2	
+1.5V	1.5V (S0, S1) 0.7A
+3.3V	3.3V (S0, S1) 1.3A
+3.3VDUAL	3.3V (S3, S5) 0.3A

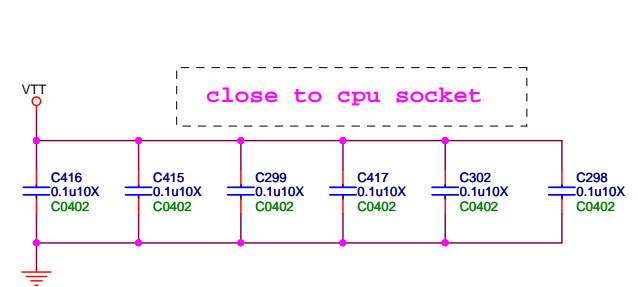
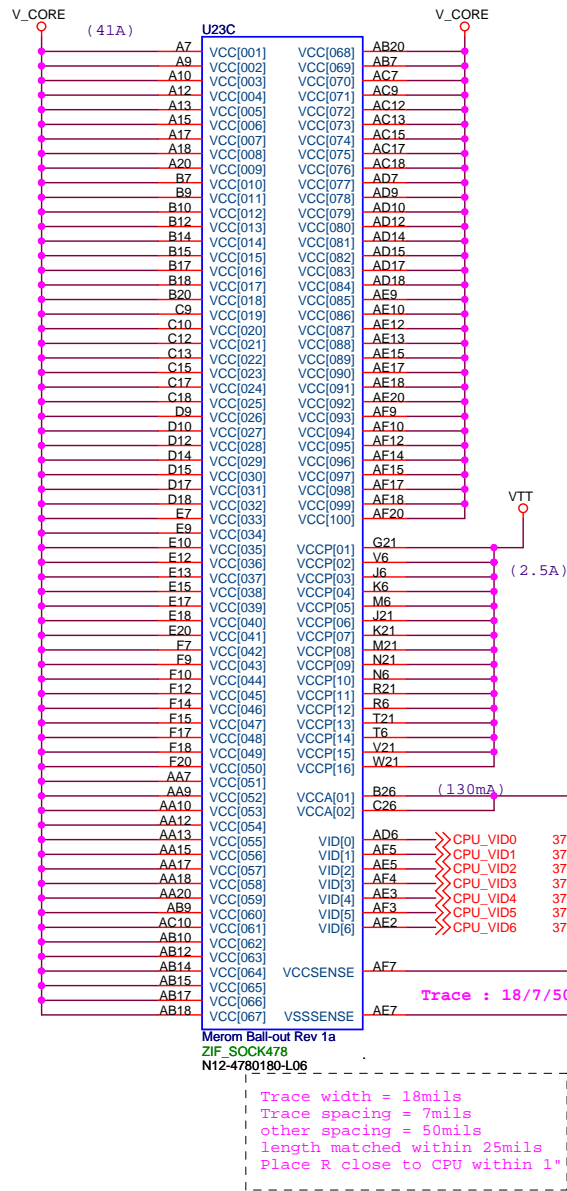
SB SB700	
+1.2V	BEAD PCIE IO 0.8A
+1.2V	BEAD PCIE PVDD 80mA
+1.2V	BEAD ATA I/O 0.2A
+1.2V	BEAD ATA PLL 0.01A
VDD33_18	3.3V OR 1.8v I/O 0.45A
+1.2V	BEAD SB CORE 0.6A
+1.2VDUAL	1.2V S5 PW 0.22A
+3.3VDUAL	3.3V S5 PW 0.01A
+3.3VDUAL	BEAD USB I/O 0.2A
+1.2VDUAL	BEAD USB CORE 0.2A
VDD33_18	

MXM HE	
MXM_EN	SW MXM_VDD_1.8V
+1.8V	SW MXM_VDD_2.5V
+2.5V	SW MXM_VDD_3.3V
+3.3V	SW MXM_VDD_5V
+5V	SW MXM_VDD_MAIN
+VIN	



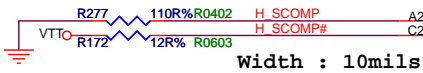






5 H_D#[63:0] >> H_D#[63:0]
 5 H_RS#[2:0] >> H_RS#[2:0]
 5 H_REQ#[4:0] >> H_REQ#[4:0]
 5 H_A#[35:3] >> H_A#[35:3]
 5 H_DINV#[3:0] >> H_DINV#[3:0]
 5 H_DSTBN#[3:0] >> H_DSTBN#[3:0]
 5 H_DSTBP#[3:0] >> H_DSTBP#[3:0]

Trace to pin within
 0.5"
 Spacing 25mils



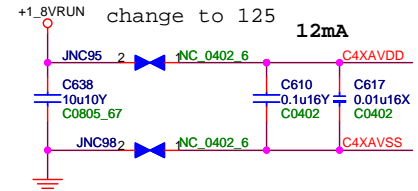
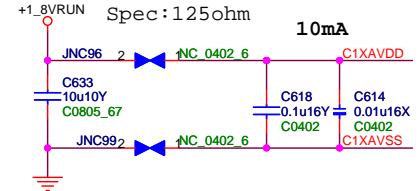
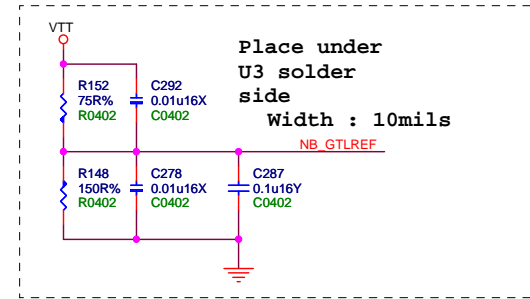
H_D#0	N29	HD0#
H_D#1	M30	HD1#
H_D#2	M28	HD2#
H_D#3	L30	HD3#
H_D#4	L29	HD4#
H_D#5	K28	HD5#
H_D#6	K31	HD6#
H_D#7	K30	HD7#
H_D#8	H31	HD8#
H_D#9	G34	HD9#
H_D#10	H32	HD10#
H_D#11	G32	HD11#
H_D#12	K32	HD12#
H_D#13	F34	HD13#
H_D#14	F33	HD14#
H_D#15	F32	HD15#
H_D#16	H28	HD16#
H_D#17	J30	HD17#
H_D#18	H30	HD18#
H_D#19	G29	HD19#
H_D#20	J29	HD20#
H_D#21	G30	HD21#
H_D#22	F30	HD22#
H_D#23	D33	HD23#
H_D#24	D34	HD24#
H_D#25	B32	HD25#
H_D#26	B33	HD26#
H_D#27	G34	HD27#
H_D#28	D31	HD28#
H_D#29	A32	HD29#
H_D#30	A31	HD30#
H_D#31	C31	HD31#
H_D#32	B30	HD32#
H_D#33	C30	HD33#
H_D#34	A30	HD34#
H_D#35	D28	HD35#
H_D#36	G28	HD36#
H_D#37	C29	HD37#
H_D#38	C28	HD38#
H_D#39	E28	HD39#
H_D#40	E27	HD40#
H_D#41	C27	HD41#
H_D#42	C26	HD42#
H_D#43	E26	HD43#
H_D#44	D26	HD44#
H_D#45	B26	HD45#
H_D#46	A26	HD46#
H_D#47	C26	HD47#
H_D#48	G22	HD48#
H_D#49	C24	HD49#
H_D#50	A25	HD50#
H_D#51	B24	HD51#
H_D#52	C25	HD52#
H_D#53	A24	HD53#
H_D#54	E23	HD54#
H_D#55	E25	HD55#
H_D#56	G24	HD56#
H_D#57	D22	HD57#
H_D#58	C22	HD58#
H_D#59	E22	HD59#
H_D#60	C23	HD60#
H_D#61	A23	HD61#
H_D#62	A22	HD62#
H_D#63	B22	HD63#
H_DINV#0	J32	DBI0#
H_DINV#1	E32	DBI1#
H_DINV#2	F27	DBI2#
H_DINV#3	F23	DBI3#
H_DSTBN#0	H33	HDSTBN0#
H_DSTBN#1	E31	HDSTBN1#
H_DSTBN#2	B28	HDSTBN2#
H_DSTBN#3	D24	HDSTBN3#
H_DSTBP#0	H34	HDSTBP0#
H_DSTBP#1	D32	HDSTBP1#
H_DSTBP#2	A28	HDSTBP2#
H_DSTBP#3	E24	HDSTBP3#
H_SCOMP	A21	HPCOMP
H_SCOMP#	C21	HNCOMP

Width : 10mils

672DX
 TEBGA847
 B01-672DX05-S22

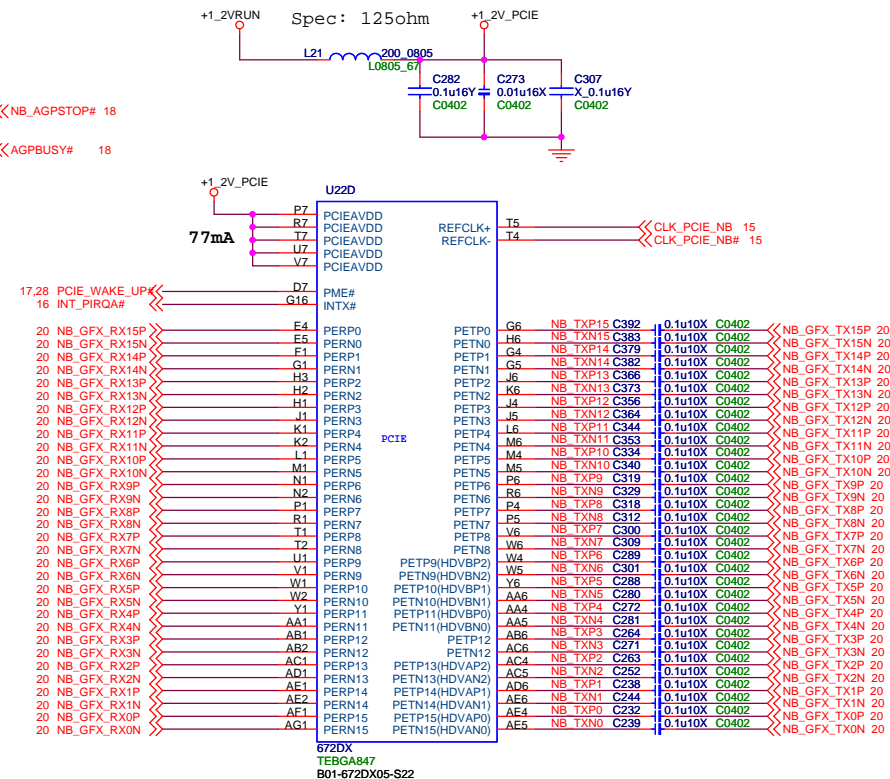
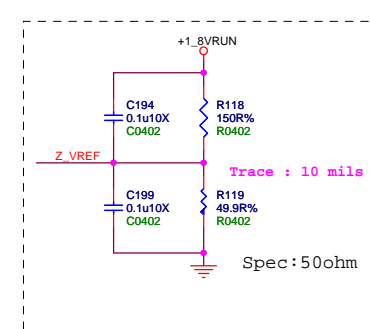
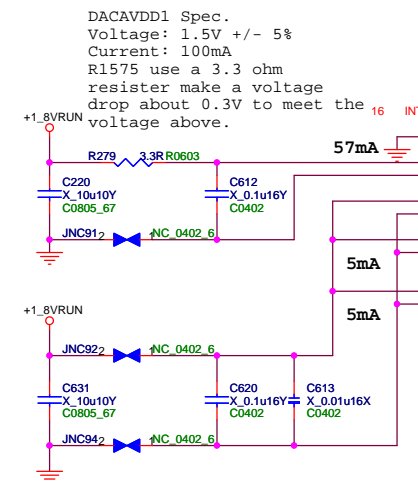
C1XAVDD	B16	C1XAVDD
C1XAVSS	C17	C1XAVSS
C4XAVDD	A17	C4XAVDD
C4XAVSS	B18	C4XAVSS
HVREF	W24	NB_GTLREF
HVREF	U24	
HVREF	R24	
HVREF	N24	
HVREF	L21	
PCREQ#	R34	TPJNC10JNC
EDRDY#	P32	TPJNC9JNC
NC	E21	
CPUCLK	F18	CLK_NB_BCLK 15
CPUCLK#	G18	CLK_NB_BCLK# 15
HLOCK#	L32	H_LOCK# 5
DEFER#	P30	H_DEFER# 5
HTRDY#	P31	H_TRDY# 5
CPURST#	F21	H_CPURST# 5
CPUPWRGD	P28	H_PWRGD 5
BPRI#	N30	H_BPRI# 5
BREQ0#	P33	H_BREQ# 5
RS0#	K34	H_RS#0
RS1#	M31	H_RS#1
RS2#	K33	H_RS#2
ADS#	M34	H_ADS# 5
HITM#	N34	H_HITM# 5
HIT#	N32	H_HIT# 5
DRDY#	M33	H_DRDY# 5
DBSY#	L34	H_DBSY# 5
BNR#	M32	H_BNR# 5
HREQ0#	T34	H_REQ#0
HREQ1#	R30	H_REQ#1
HREQ2#	R29	H_REQ#2
HREQ3#	R32	H_REQ#3
HREQ4#	P34	H_REQ#4
HASTB0#	U34	H_ASTB#0 5
HASTB1#	AA34	H_ASTB#1 5
HA3#	T32	H_A#3
HA4#	T28	H_A#4
HA5#	T31	H_A#5
HA6#	T33	H_A#6
HA7#	T30	H_A#7
HA8#	U32	H_A#8
HA9#	U30	H_A#9
HA10#	V34	H_A#10
HA11#	U29	H_A#11
HA12#	V33	H_A#12
HA13#	V32	H_A#13
HA14#	V28	H_A#14
HA15#	V31	H_A#15
HA16#	W34	H_A#16
HA17#	W32	H_A#17
HA18#	W33	H_A#18
HA19#	V30	H_A#19
HA20#	Y34	H_A#20
HA21#	Y28	H_A#21
HA22#	W29	H_A#22
HA23#	Y32	H_A#23
HA24#	Y30	H_A#24
HA25#	Y31	H_A#25
HA26#	AA32	H_A#26
HA27#	AA30	H_A#27
HA28#	AA29	H_A#28
HA29#	AB33	H_A#29
HA30#	AB34	H_A#30
HA31#	AB32	H_A#31
HA32#	AC34	H_A#32
HA33#	AB30	H_A#33
HA34#	AB31	H_A#34
HA35#		H_A#35

HVREF signal should be kept away from high-speed signals to prevent crosstalk.



Width : 15mils

		MICRO-STAR INT'L CO.,LTD.	
772DX (HOST BUS)			
Size	Document Number		Rev
B	MS-1452		0A
Date:	Monday, March 23, 2009	Sheet	7 of 49



U22B		
M A DQ0	AD31	MD0A
M A DQ1	AD30	MD1A
M A DQ2	AG34	MD2A
M A DQ3	AE29	MD3A
M A DQ4	AE32	MD4A
M A DQ5	AE34	MD5A
M A DQ6	AE31	MD6A
M A DQ7	AE30	MD7A
M A DM0	AD28	DOM0A
M A DQS0	AF32	DQS0A
M A DQS#0	AF33	DQS0A#
M A DQ8	AF28	MD8A
M A DQ9	AJ34	MD9A
M A DQ10	AH31	MD10A
M A DQ11	AG30	MD11A
M A DQ12	AG32	MD12A
M A DQ13	AG32	MD13A
M A DQ14	AJ32	MD14A
M A DQ15	AJ31	MD15A
M A DM1	AH34	DOM1A
M A DQS1	AH32	DQS1A
M A DQS#1	AH33	DQS1A#
M A DQ16	AK34	MD16A
M A DQ17	AH30	MD17A
M A DQ18	AL32	MD18A
M A DQ19	AM33	MD19A
M A DQ20	AK32	MD20A
M A DQ21	AG29	MD21A
M A DQ22	AM34	MD22A
M A DQ23	AL31	MD23A
M A DM2	AJ30	DOM2A
M A DQS2	AK33	DQS2A
M A DQS#2	AK34	DQS2A#
M A DQ24	AM32	MD24A
M A DQ25	AP32	MD25A
M A DQ26	AP31	MD26A
M A DQ27	AM29	MD27A
M A DQ28	AK30	MD28A
M A DQ29	AK29	MD29A
M A DQ30	AJ27	MD30A
M A DQ31	AK28	MD31A
M A DM3	AN32	DQM3A
M A DQS3	AM30	DQS3A
M A DQS#3	AM31	DQS3A#
M A DQ32	AK20	MD32A
M A DQ33	AM20	MD33A
M A DQ34	AM19	MD34A
M A DQ35	AJ19	MD35A
M A DQ36	AN20	MD36A
M A DQ37	AJ21	MD37A
M A DQ38	AP19	MD38A
M A DQ39	AH20	MD39A
M A DM4	AK21	DQM4A
M A DQS4	AK19	DQS4A
M A DQS#4	AL19	DQS4A#
M A DQ40	AK18	MD40A
M A DQ41	AJ17	MD41A
M A DQ42	AK17	MD42A
M A DQ43	AP16	MD43A
M A DQ44	AH18	MD44A
M A DQ45	AP18	MD45A
M A DQ46	AN18	MD46A
M A DQ47	AP17	MD47A
M A DM5	AM18	DQM5A
M A DQS5	AL17	DQS5A
M A DQS#5	AM17	DQS5A#
M A DQ48	AN16	MD48A
M A DQ49	AK16	MD49A
M A DQ50	AN14	MD50A
M A DQ51	AJ15	MD51A
M A DQ52	AP15	MD52A
M A DQ53	AM16	MD53A
M A DQ54	AK15	MD54A
M A DQ55	AP14	MD55A
M A DM6	AH16	DQM6A
M A DQS6	AL15	DQS6A
M A DQS#6	AM15	DQS6A#
M A DQ56	AL13	MD56A
M A DQ57	AM13	MD57A
M A DQ58	AM12	MD58A
M A DQ59	AJ13	MD59A
M A DQ60	AM14	MD60A
M A DQ61	AK14	MD61A
M A DQ62	AN12	MD62A
M A DQ63	AH14	MD63A
M A DM7	AK13	DQM7A
M A DQS7	AP12	DQS7A
M A DQS#7	AP13	DQS7A#

DRAM

FWSDSCLKOA
FWSDSCLKOA#

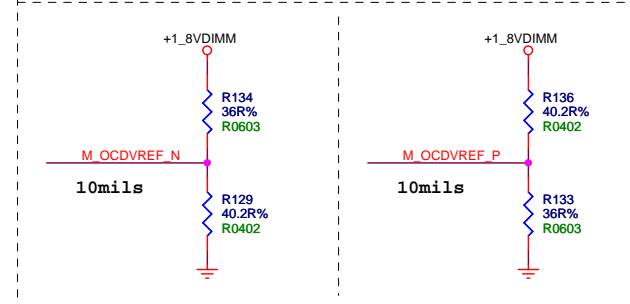
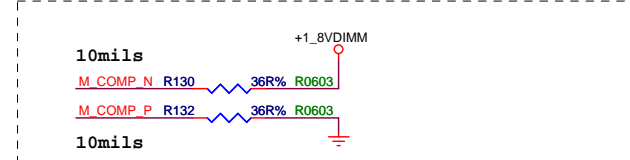
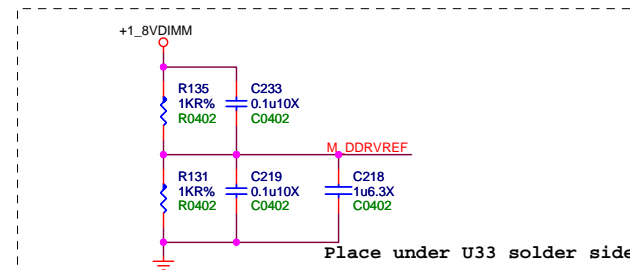
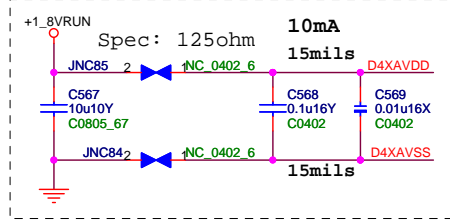
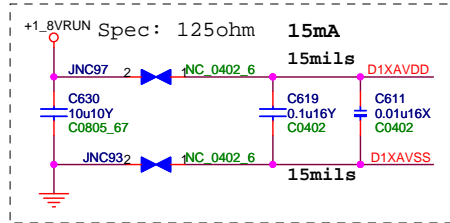
DDRVREF0
DDRVREF1

DDRCOMP
DDRCOMN

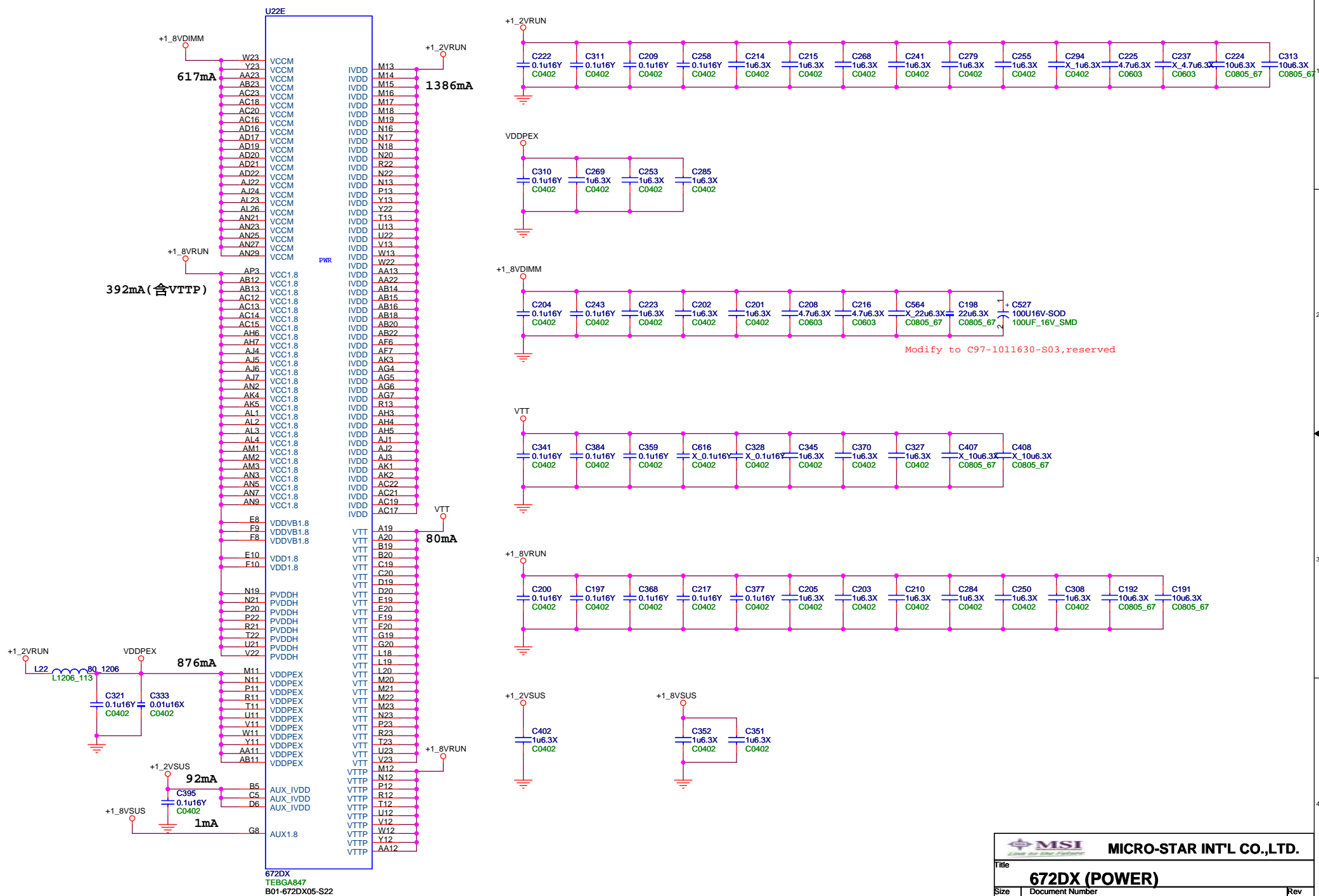
OCDVREFP
OCDVREFN

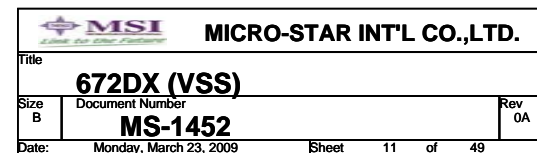
S3AUXSW#

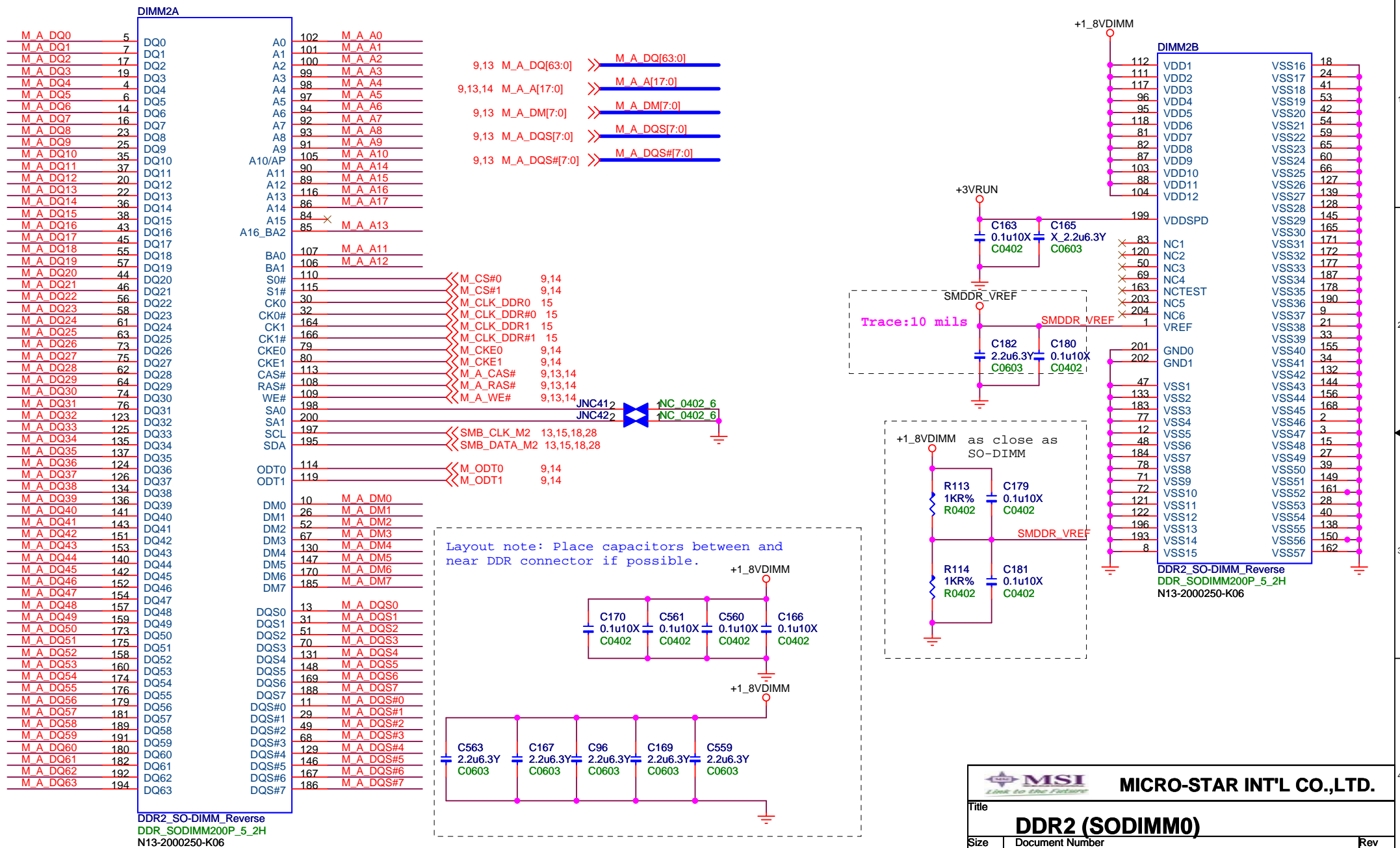
A15	D1XAVDD	12,13	M_A_DQ[63:0]	>>	M_A_DQ[63:0]
B15	D1XAVSS	12,13,14	M_A_A[17:0]	>>	M_A_A[17:0]
AP11	D4XAVDD	12,13	M_A_DM[7:0]	>>	M_A_DM[7:0]
AP10	D4XAVSS	12,13	M_A_DQS[7:0]	>>	M_A_DQS[7:0]
		12,13	M_A_DQS#[7:0]	>>	M_A_DQS#[7:0]
AH24	M_A_A0				
AP25	M_A_A1				
AM25	M_A_A2				
AL25	M_A_A3				
AP26	M_A_A4				
AM26	M_A_A5				
AN26	M_A_A6				
AK25	M_A_A7				
AP27	M_A_A8				
AP28	M_A_A9				
AK24	M_A_A10				
AN24	M_A_A11				
AP24	M_A_A12				
AM28	M_A_A13				
AM27	M_A_A14				
AN28	M_A_A15				
AP21	M_A_A16				
AP29	M_A_A17				
AM23	M_A_RAS#	12,13,14			
AP22	M_A_CAS#	12,13,14			
AJ23	M_A_WE#	12,13,14			
AK12	FWSDSCLKOA	JNC532	>>	M_FWSDSCLKOA	15
AH12	FWSDSCLKOA#	JNC482	>>	M_FWSDSCLKOA#	15
AP23	M_CS#0	12,14			
AH22	M_CS#1	12,14			
AM22	M_CS#2	13,14			
AM21	M_CS#3	13,14			
AK22	M_ODT0	12,14			
AP20	M_ODT1	12,14			
AN22	M_ODT2	13,14			
AL21	M_ODT3	13,14			
AN30	M_CKE0	12,14			
AP30	M_CKE1	12,14			
AH26	M_CKE2	13,14			
AK27	M_CKE3	13,14			
AD18	M_DDRVREF				
AD23					
AJ25	M_COMP_P				
AK26	M_COMP_N				
AH28	M_OCDVREF_P				
AJ29	M_OCDVREF_N				
B6	TPJNC17JNC				



1. check power consumption of every power group







DIMM1A		
M_A DQ0	5	DQ0
M_A DQ1	7	DQ1
M_A DQ2	17	DQ2
M_A DQ3	19	DQ3
M_A DQ4	4	DQ4
M_A DQ5	6	DQ5
M_A DQ6	14	DQ6
M_A DQ7	16	DQ7
M_A DQ8	23	DQ8
M_A DQ9	25	DQ9
M_A DQ10	35	DQ10
M_A DQ11	37	DQ11
M_A DQ12	20	DQ12
M_A DQ13	22	DQ13
M_A DQ14	36	DQ14
M_A DQ15	38	DQ15
M_A DQ16	43	DQ16
M_A DQ17	45	DQ17
M_A DQ18	55	DQ18
M_A DQ19	57	DQ19
M_A DQ20	44	DQ20
M_A DQ21	46	DQ21
M_A DQ22	56	DQ22
M_A DQ23	58	DQ23
M_A DQ24	61	DQ24
M_A DQ25	63	DQ25
M_A DQ26	73	DQ26
M_A DQ27	75	DQ27
M_A DQ28	62	DQ28
M_A DQ29	64	DQ29
M_A DQ30	74	DQ30
M_A DQ31	76	DQ31
M_A DQ32	123	DQ32
M_A DQ33	125	DQ33
M_A DQ34	135	DQ34
M_A DQ35	137	DQ35
M_A DQ36	124	DQ36
M_A DQ37	126	DQ37
M_A DQ38	134	DQ38
M_A DQ39	136	DQ39
M_A DQ40	141	DQ40
M_A DQ41	143	DQ41
M_A DQ42	151	DQ42
M_A DQ43	153	DQ43
M_A DQ44	140	DQ44
M_A DQ45	142	DQ45
M_A DQ46	152	DQ46
M_A DQ47	154	DQ47
M_A DQ48	157	DQ48
M_A DQ49	159	DQ49
M_A DQ50	173	DQ50
M_A DQ51	175	DQ51
M_A DQ52	158	DQ52
M_A DQ53	160	DQ53
M_A DQ54	174	DQ54
M_A DQ55	176	DQ55
M_A DQ56	179	DQ56
M_A DQ57	181	DQ57
M_A DQ58	189	DQ58
M_A DQ59	191	DQ59
M_A DQ60	180	DQ60
M_A DQ61	182	DQ61
M_A DQ62	192	DQ62
M_A DQ63	194	DQ63

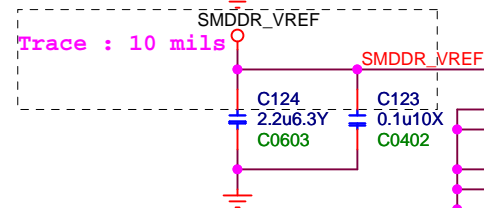
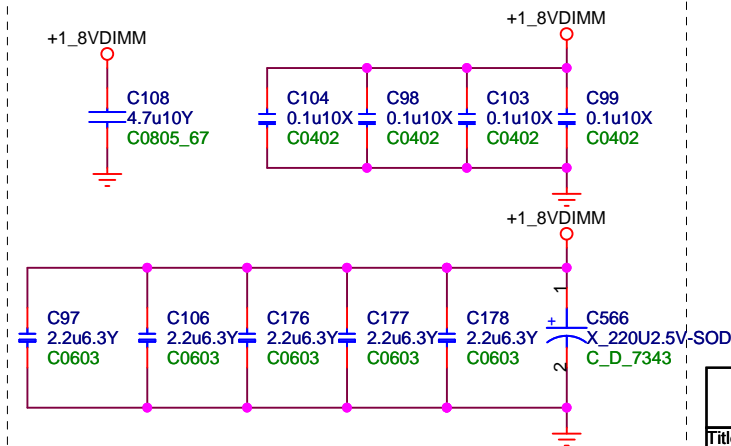
DDR2-Reverse_9.2H
DDR_SODIMM200P_9_2H
N13-2000400-K06

DIMM1B		
A0	102	M_A A0
A1	101	M_A A1
A2	100	M_A A2
A3	99	M_A A3
A4	98	M_A A4
A5	97	M_A A5
A6	94	M_A A6
A7	92	M_A A7
A8	93	M_A A8
A9	91	M_A A9
A10/AP	105	M_A A10
A11	90	M_A A14
A12	89	M_A A15
A13	116	M_A A16
A14	86	M_A A17
A15	84	M_A A13
A16_BA2	85	M_A A13
BA0	107	M_A A11
BA1	106	M_A A12
S0#	110	
S1#	115	
CK0	30	
CK0#	32	
CK1	164	
CK1#	166	
CKE0	79	
CKE1	80	
CAS#	113	
RAS#	108	
WE#	109	
SA0	198	
SA1	200	
SCL	197	
SDA	195	
ODT0	114	
ODT1	119	
DM0	10	M_A DM0
DM1	26	M_A DM1
DM2	52	M_A DM2
DM3	67	M_A DM3
DM4	130	M_A DM4
DM5	147	M_A DM5
DM6	170	M_A DM6
DM7	185	M_A DM7
DQS0	13	M_A DQS0
DQS1	31	M_A DQS1
DQS2	51	M_A DQS2
DQS3	70	M_A DQS3
DQS4	131	M_A DQS4
DQS5	148	M_A DQS5
DQS6	169	M_A DQS6
DQS7	188	M_A DQS7
DQS#0	11	M_A DQS#0
DQS#1	29	M_A DQS#1
DQS#2	49	M_A DQS#2
DQS#3	68	M_A DQS#3
DQS#4	129	M_A DQS#4
DQS#5	146	M_A DQS#5
DQS#6	167	M_A DQS#6
DQS#7	186	M_A DQS#7

9,12 M_A_DQ[63:0] >> M_A_DQ[63:0]
9,12,14 M_A_A[17:0] >> M_A_A[17:0]
9,12 M_A_DM[7:0] >> M_A_DM[7:0]
9,12 M_A_DQS[7:0] >> M_A_DQS[7:0]
9,12 M_A_DQS#[7:0] >> M_A_DQS#[7:0]

M_CS#2 9,14
M_CS#3 9,14
M_CLK_DDR2 15
M_CLK_DDR2# 15
M_CLK_DDR3 15
M_CLK_DDR3# 15
M_CKE2 9,14
M_CKE3 9,14
M_A_CAS# 9,12,14
M_A_RAS# 9,12,14
M_A_WE# 9,12,14
SMB_CLK_M2 12,15,18,28
SMB_DATA_M2 12,15,18,28
M_ODT2 9,14
M_ODT3 9,14

Layout note: Place capacitors between and near DDR connector if possible.



DIMM1B		
VDD1	112	VSS16
VDD2	111	VSS17
VDD3	117	VSS18
VDD4	96	VSS19
VDD5	95	VSS20
VDD6	118	VSS21
VDD7	81	VSS22
VDD8	82	VSS23
VDD9	87	VSS24
VDD10	103	VSS25
VDD11	88	VSS26
VDD12	104	VSS27
VDDSPD	199	VSS28
NC1	83	VSS29
NC2	120	VSS30
NC3	50	VSS31
NC4	69	VSS32
NCTEST	163	VSS33
NC5	203	VSS34
NC6	204	VSS35
VREF	1	VSS36
GND0	201	VSS37
GND1	202	VSS38
VSS1	47	VSS39
VSS2	133	VSS40
VSS3	183	VSS41
VSS4	77	VSS42
VSS5	12	VSS43
VSS6	48	VSS44
VSS7	184	VSS45
VSS8	78	VSS46
VSS9	71	VSS47
VSS10	72	VSS48
VSS11	121	VSS49
VSS12	122	VSS50
VSS13	196	VSS51
VSS14	193	VSS52
VSS15	8	VSS53
		VSS54
		VSS55
		VSS56
		VSS57

DDR2-Reverse_9.2H
DDR_SODIMM200P_9_2H
N13-2000400-K06

MICRO-STAR INT'L CO.,LTD.

DDR2 (SODIMM1)

Size

Custom

Document Number

MS-1452

Date:

Monday, March 23, 2009

Sheet

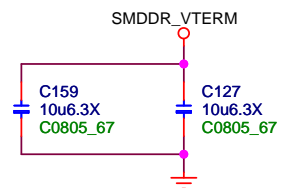
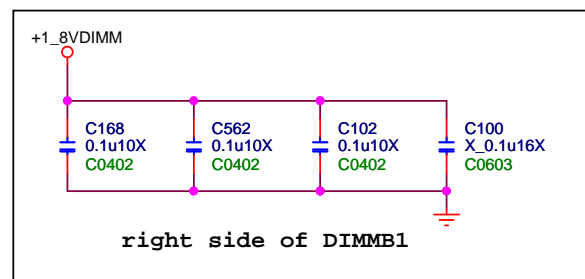
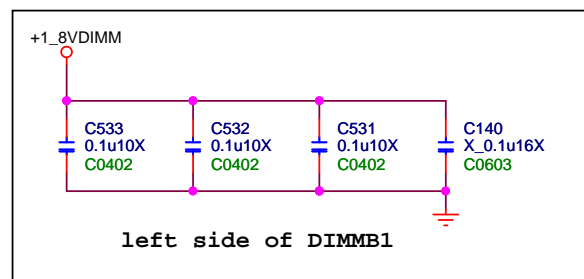
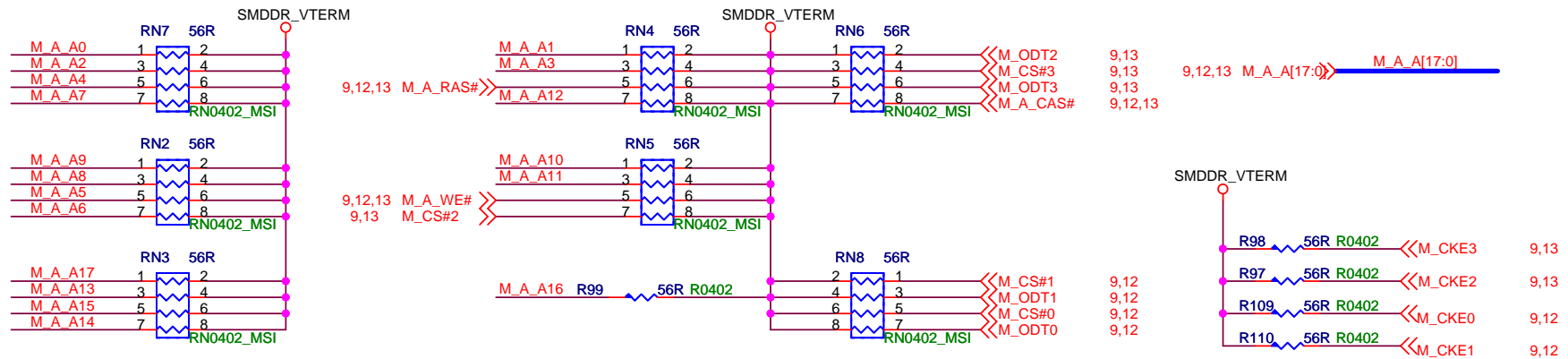
13

of

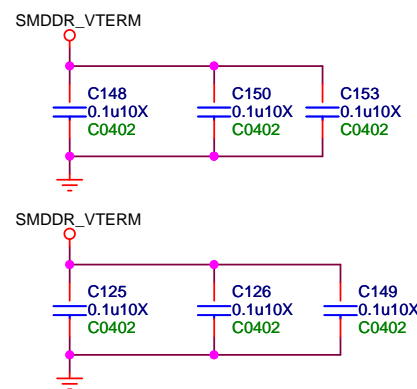
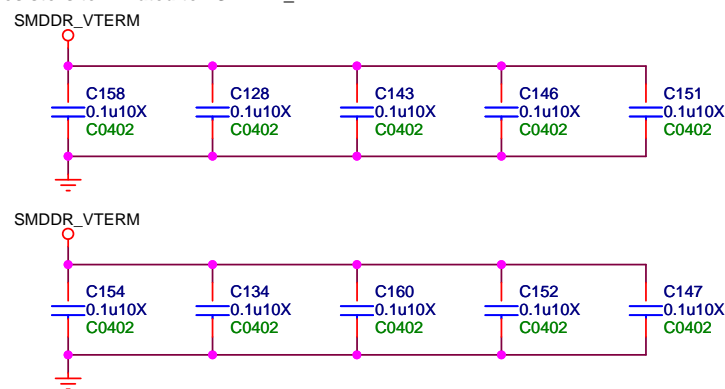
49

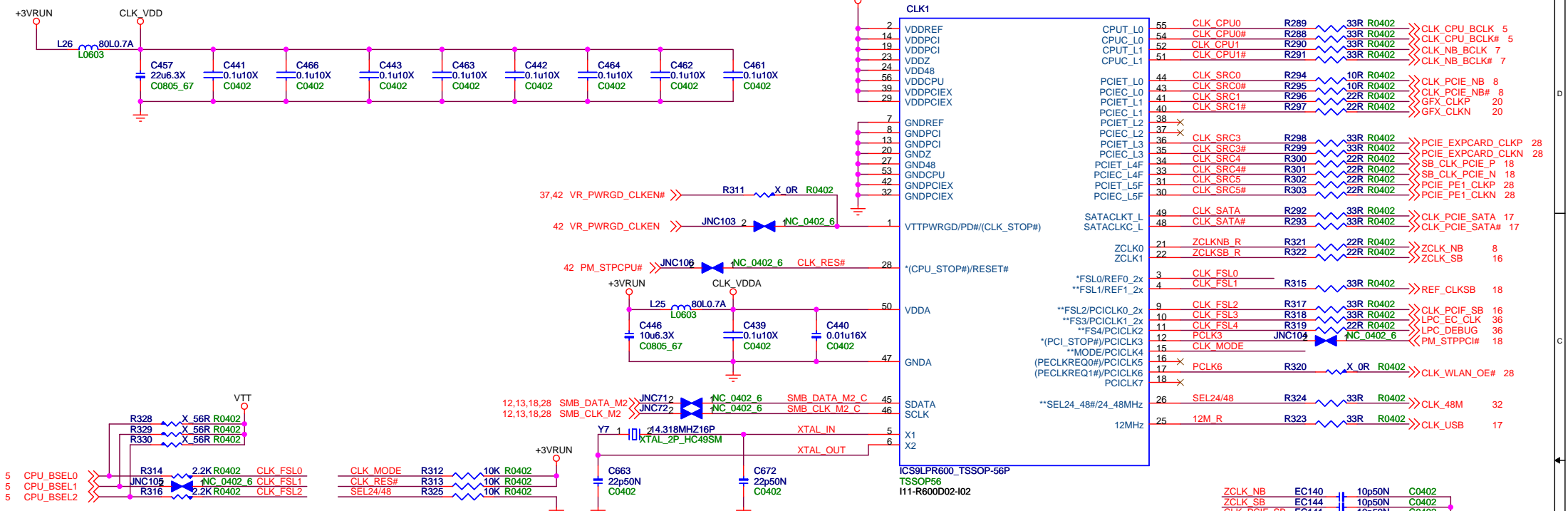
Rev

0A



Layout note: Place one cap close to every 2 pullup resistors terminated to +SMDDR_VTERN.

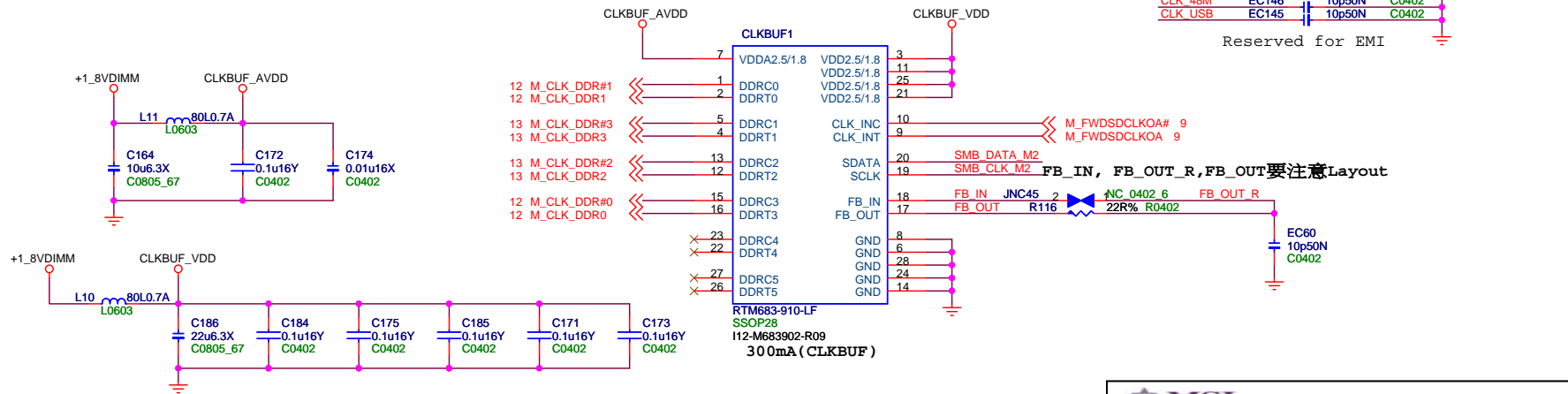





Strapping Configuration(ICS)

PIN#	High	Low(Default)
15	Pin 16/17 : PECLKREQ	Pin 16/17 : PCICLK

CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz
L	L	L	1066 MHz



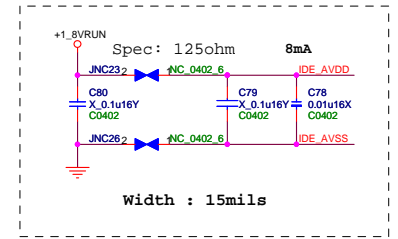
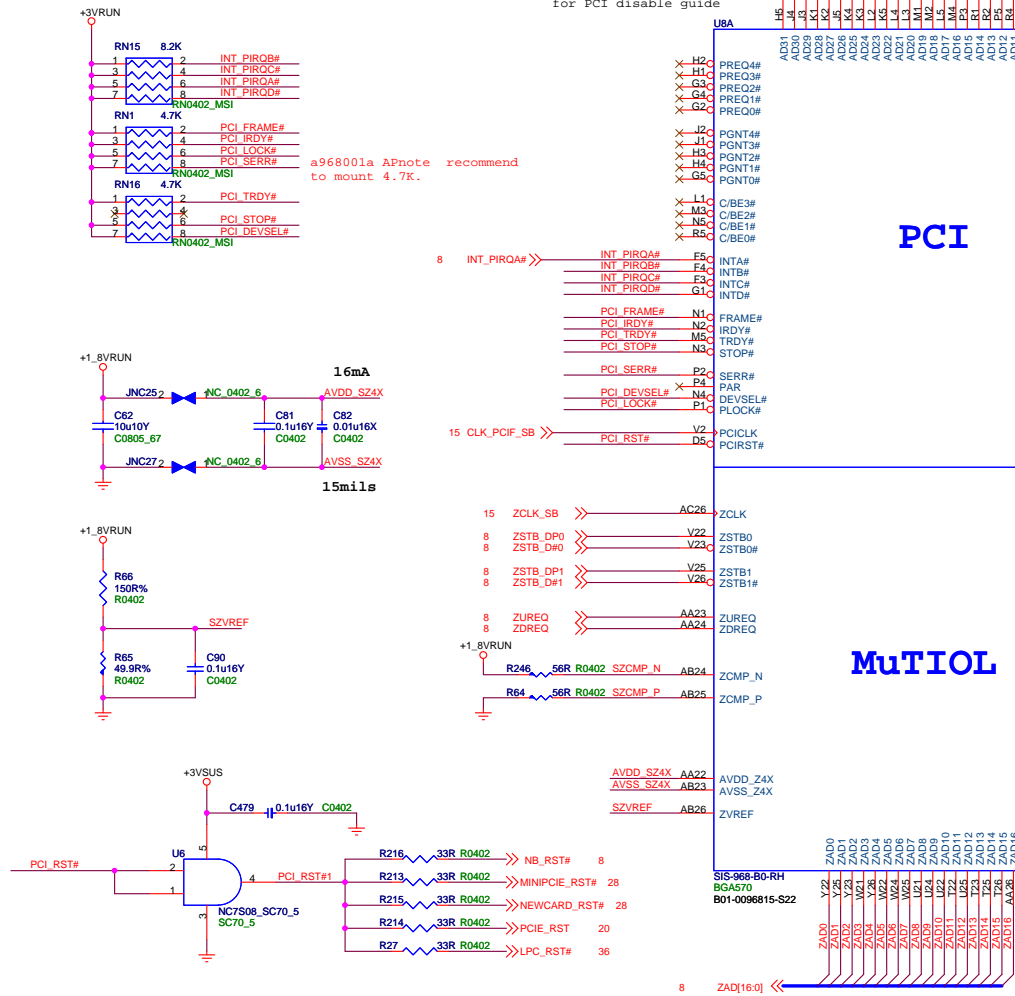
**MICRO-STAR INT'L CO.,LTD.**

Title**CLOCK (CLK GEN & DIMM BUF)**

Size B Document Number**MS-1452** Rev 0A

Date: Monday, March 23, 2009 Sheet 15 of 49

Refer to a968001a APnote
for PCI disable guide



SIS pull high to 5VRUN

SIS pull low

SIS pull low

TPJNC30

TPJNC30

TPJNC30

TPJNC30

TPJNC30

TPJNC30

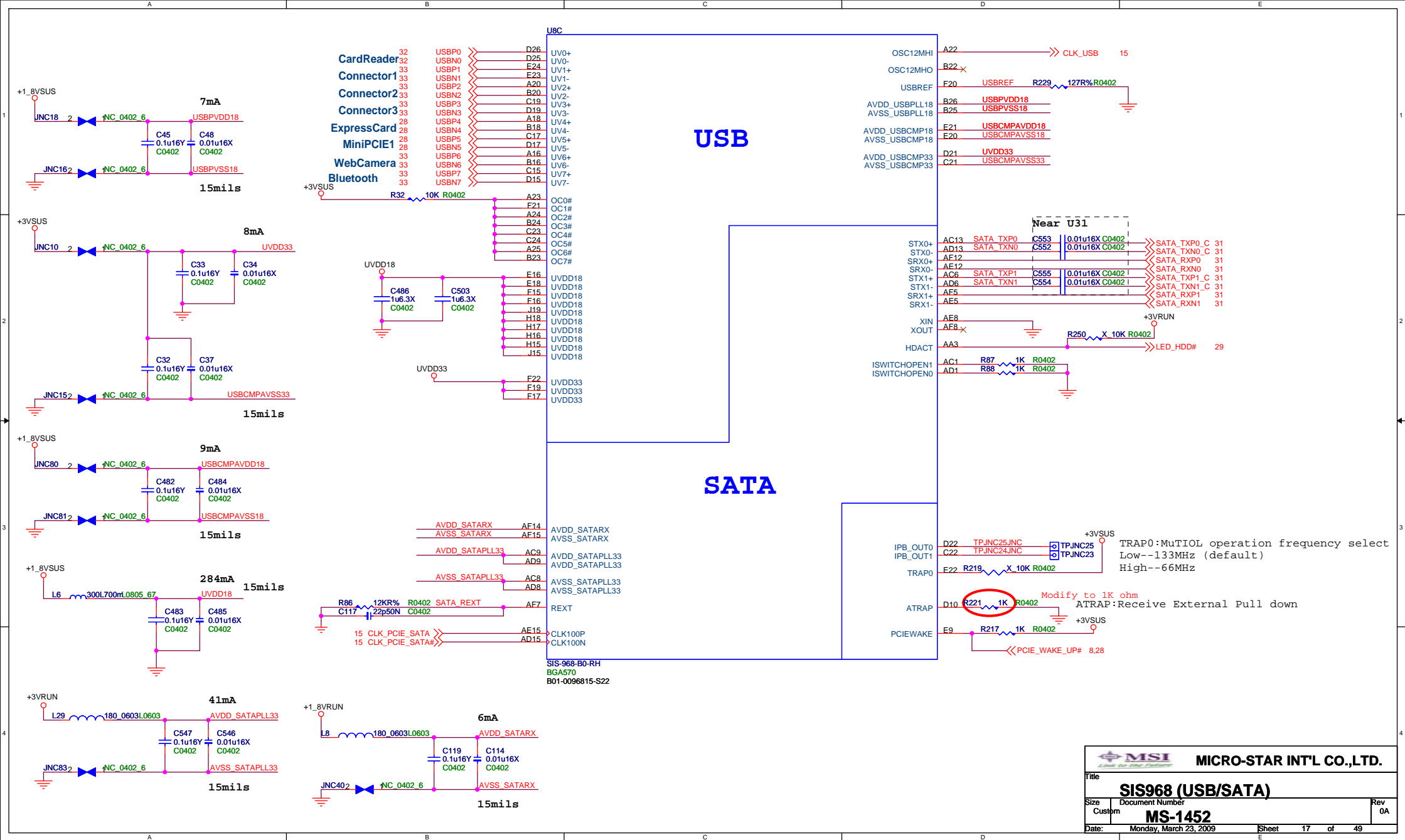
TPJNC30

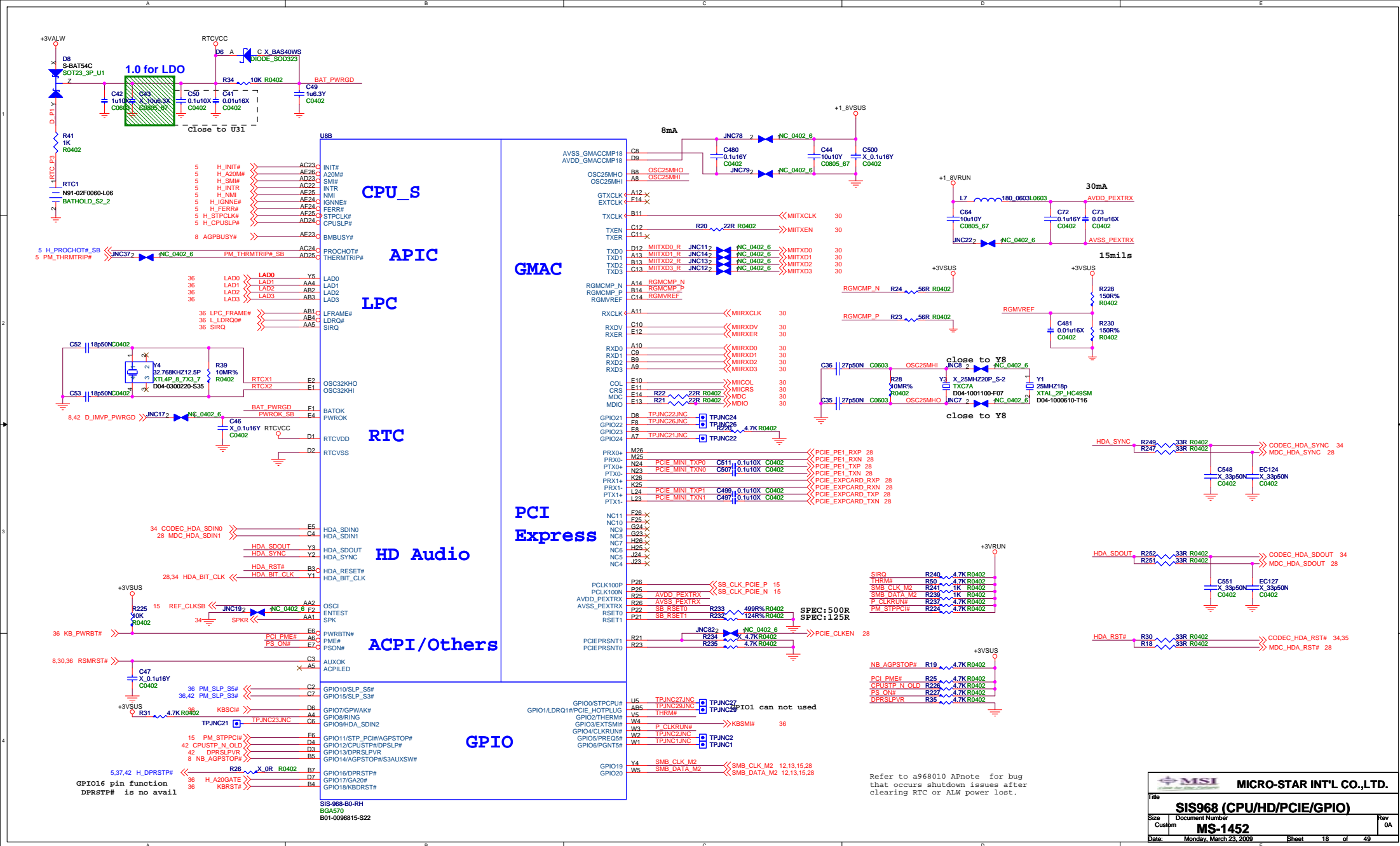
TPJNC30

TPJNC30

TPJNC30


TPJNC30

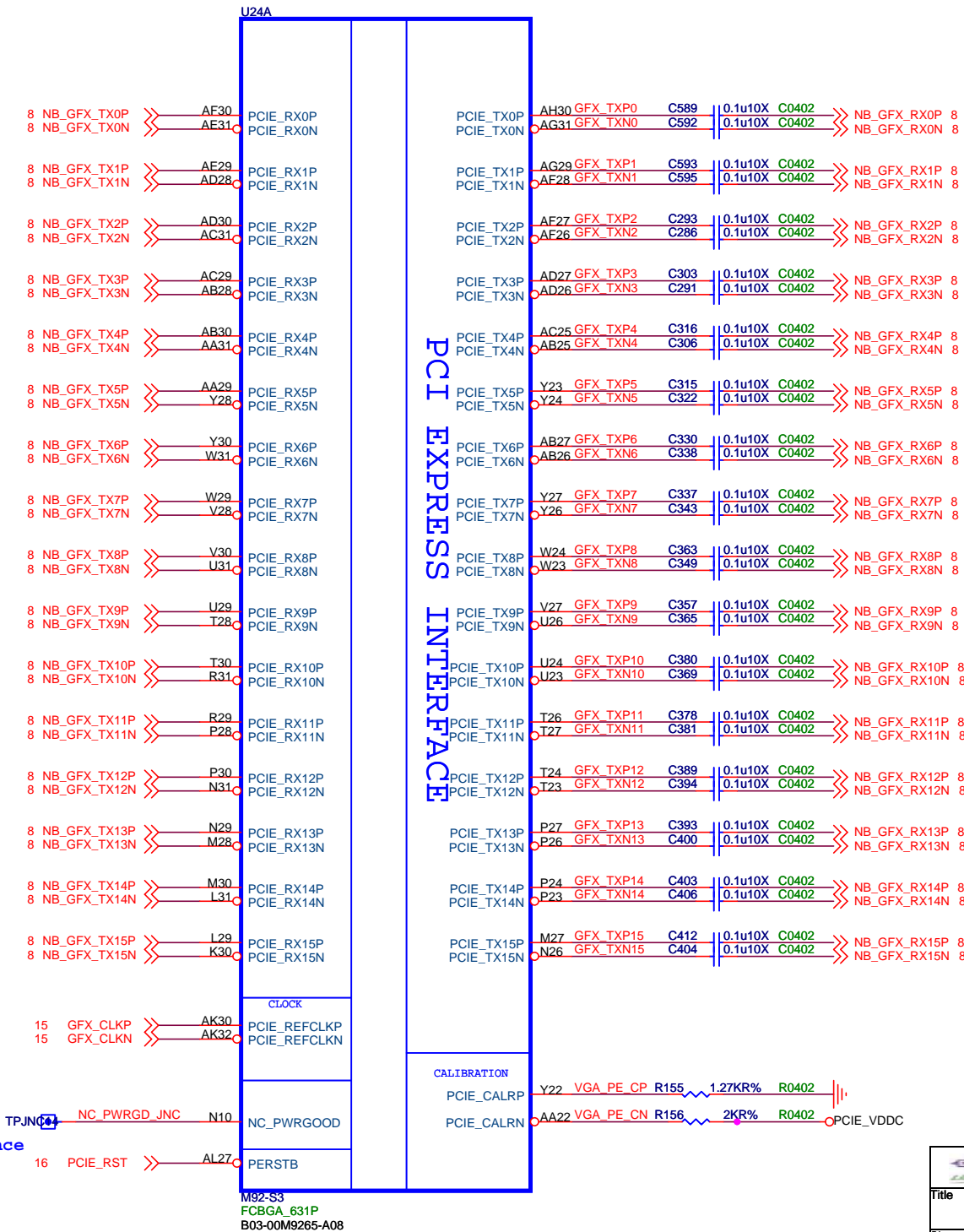


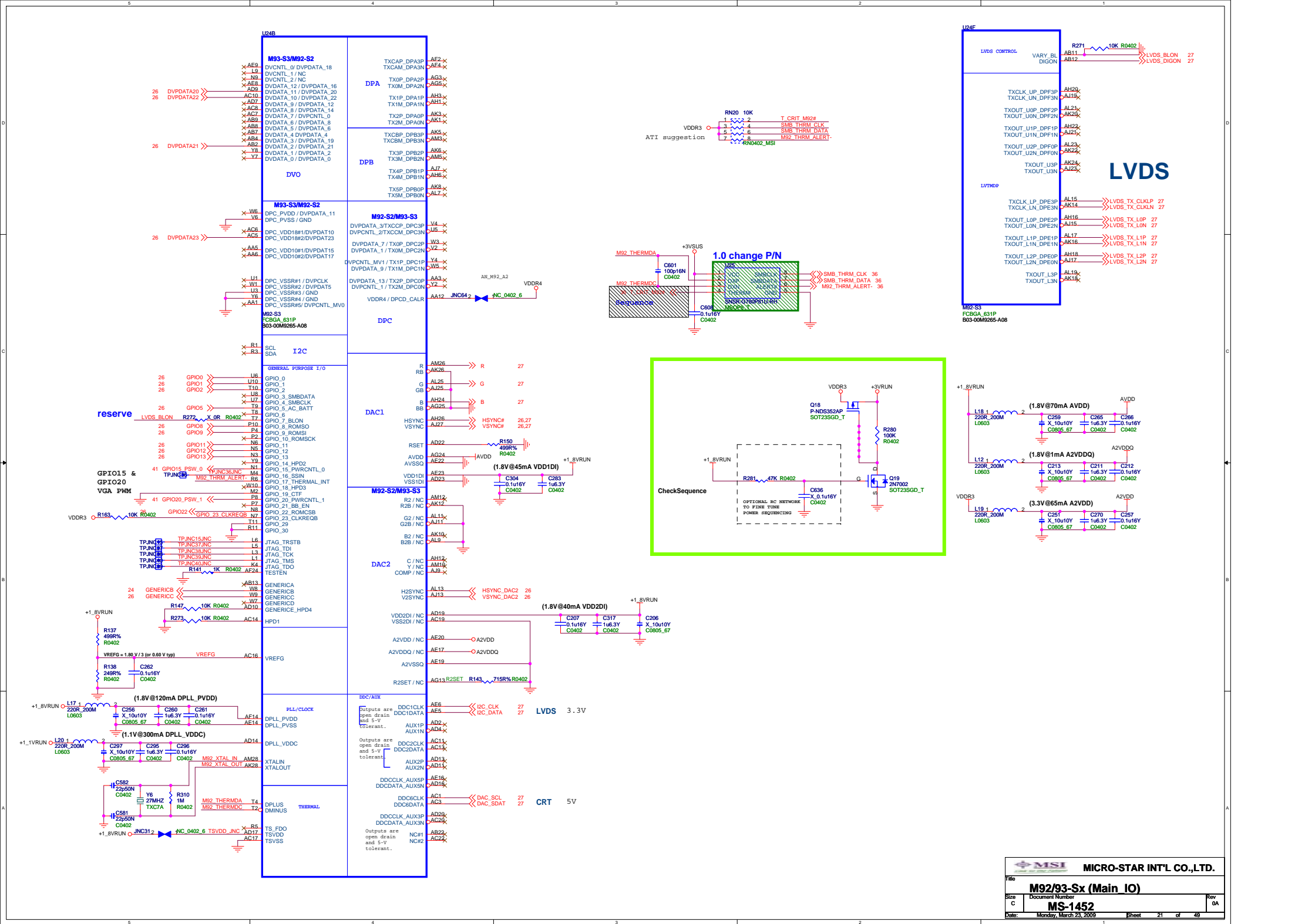


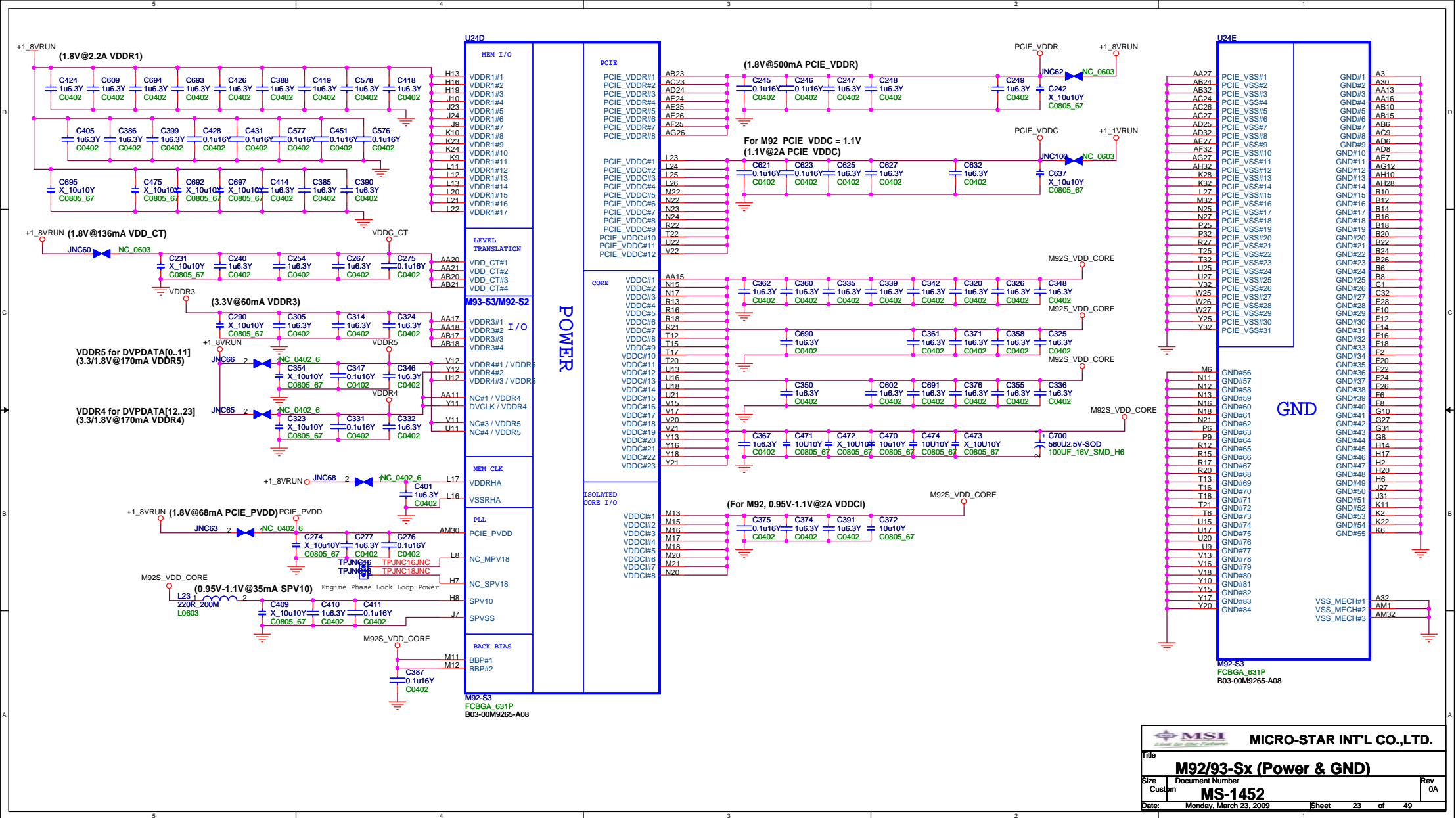
CheckResetSequence

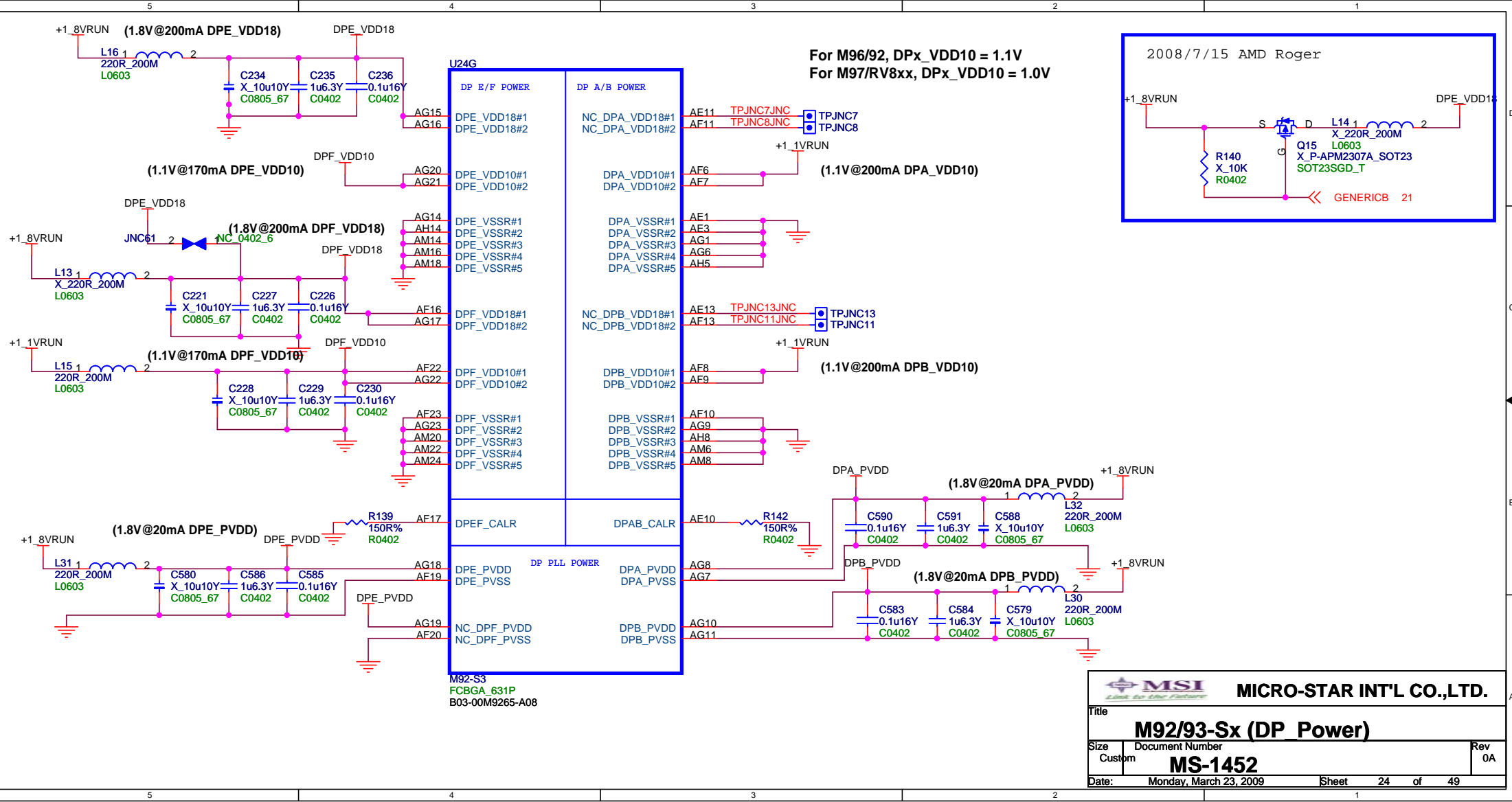
PCI EXPRESS INTERFACE

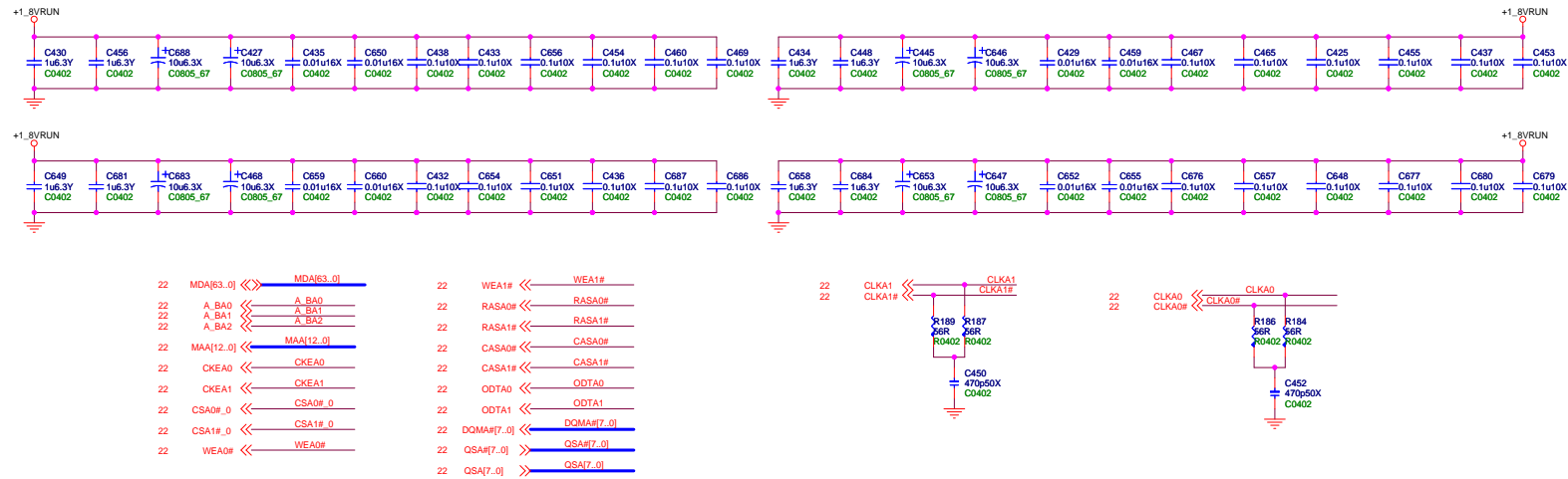
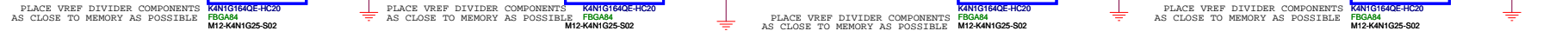
			MICRO-STAR INT'L CO.,LTD.		
Title M92/93-Sx (PCIe Interface)					
Size Custom	Document Number MS-1452				Rev 0A
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GPIO0
Transmitter Power Savings Enable
0: 50% Tx output swing
Note: This setting can only be used if the PCIe bus Design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.)
1: Full Tx output swing

GPIO1
PCI Express Transmitter De-emphasis Enable
0: Tx de-emphasis disabled
1: Tx de-emphasis enabled

GPIO2
0 = Advertises the PCIe device as 2.5 GT/s capable at power-on.
1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.
Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CBB (compliance base board).

GPIO9
VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space):
0 - VGA Controller capacity enabled
1 - The device will not be recognized as the system's VGA controller

HSYNC VSYNC
AUD[1:0]:
00 - No audio function;
01 - Audio for DisplayPort and HDMI if adapter is detected;
10 - Audio for DisplayPort only;
11 - Audio for both DisplayPort and HDMI.
HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

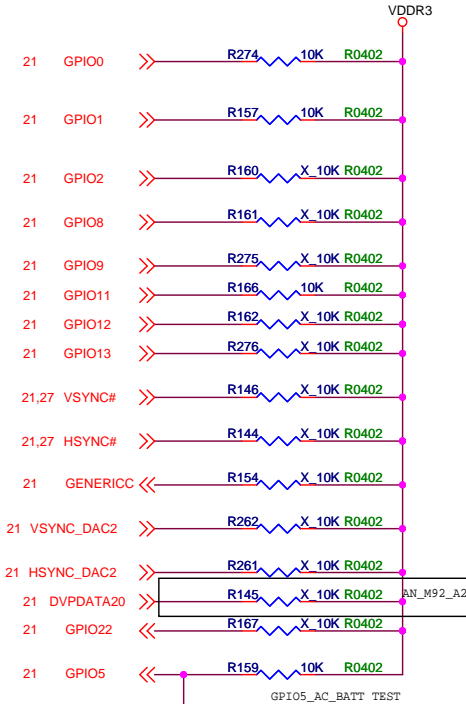
V2SYNC
VIP Device Strap Enable indicates to the software driver that it should try to sense whether or not a VIP device is connected on the VIP Host interface.
0 - Driver would ignore the value sampled on DVPDATA_20 during reset.
1 - Driver would use the sampled value sampled at reset from DVPDATA_20 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (0 indicates yes, 1 indicates no). According to the VIP 1.1 standard, DVPDATA_20 is tied high, and VIP slave devices are required to drive this signal low during reset. This scheme allows for a VIP device to be connected to the graphics adapter via a daughter card.
Note:
If the strap is needed, it must be placed between the ball and the VSYNC output buffer. This output buffer prevents monitors from affecting the value at reset.

Size of the primary memory apertures	GPIO 13 12 11
128 MB	000
256 MB	001
64 MB	010
512 MB	011
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

Due to memory bandwidth constraints, the aperture size should be set to 512 MB or less. For memory buffers larger than 512 MB (e.g. 512 MB, 1 GB) the aperture size should be 512 MB.

DVPDATA23 R420	DVPDATA22 R423	DVPDATA21 R427	MEM_TYPE
0	0	0	SAMSUNG 64MX16
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

STRAPS



36,43,44 AC_OK#>>>



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 X X


AMD RESERVED CONFIGURATION STRAPS

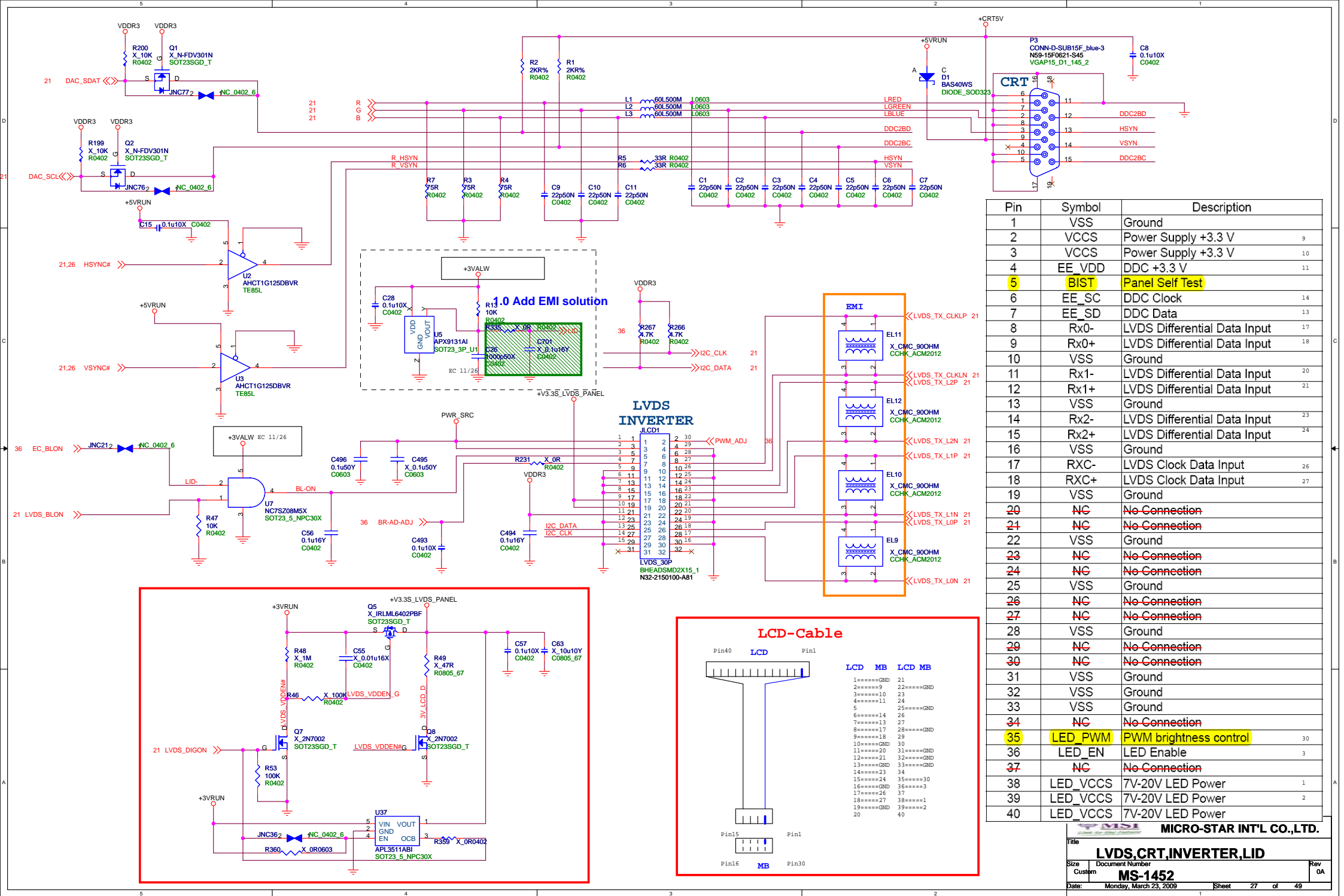
ALLOW FOR PULLUP PADS FOR THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

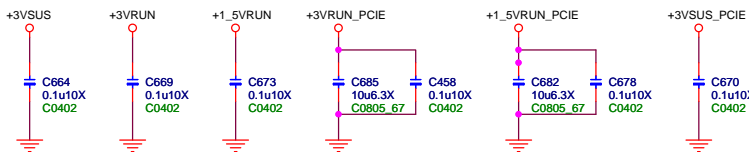
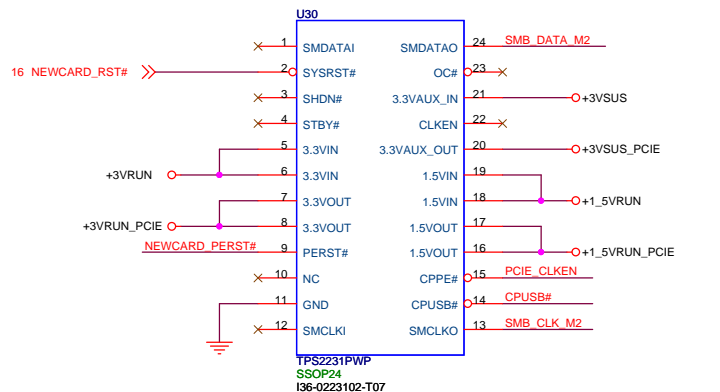
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

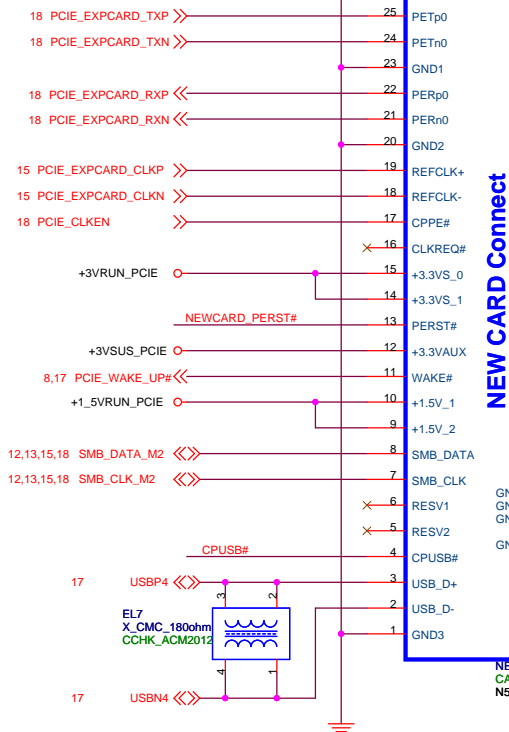
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Title M92/93-Sx (Straps & Thermal)			
Size Custom	Document Number MS-1452		Rev 0A
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NEW CARD Power Control IC
 TI : TPS2231 : 0.3415727017
 ENE : PS2231 : 0.402274502



EXPRESS CARD

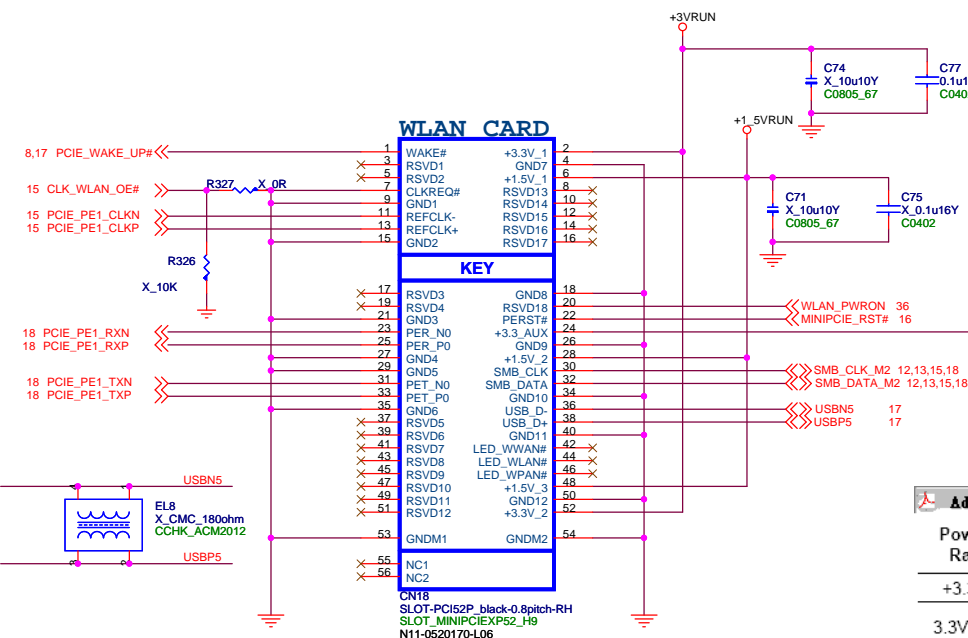


NEW CARD Connect

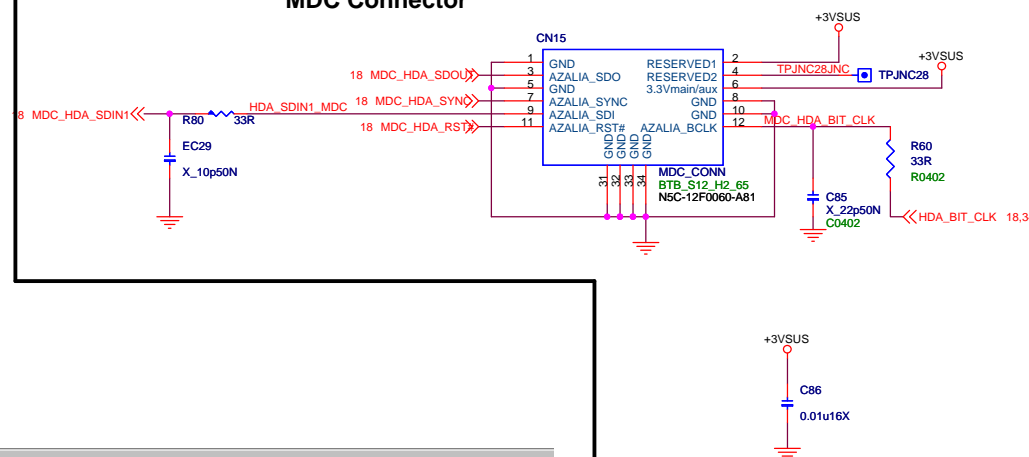
Adobe Acrobat Professional - [ExpressCard WP.pdf]

ExpressCard module power supply limits

Supply	Limits	Notes
+3.3V ¹	1000 mA – Average 1300 mA – Max	Primary supply voltage
+3.3VAUX ¹	250 mA – Average 275 mA – Max	Auxiliary supply voltage; this current is also available during the power saving D3 state with wakeup enabled
	5 mA – Average	Auxiliary supply voltage during the power saving D3 state with wakeup disabled
+1.5V	500 mA – Average 650 mA – Max	Secondary supply voltage



MDC Connector



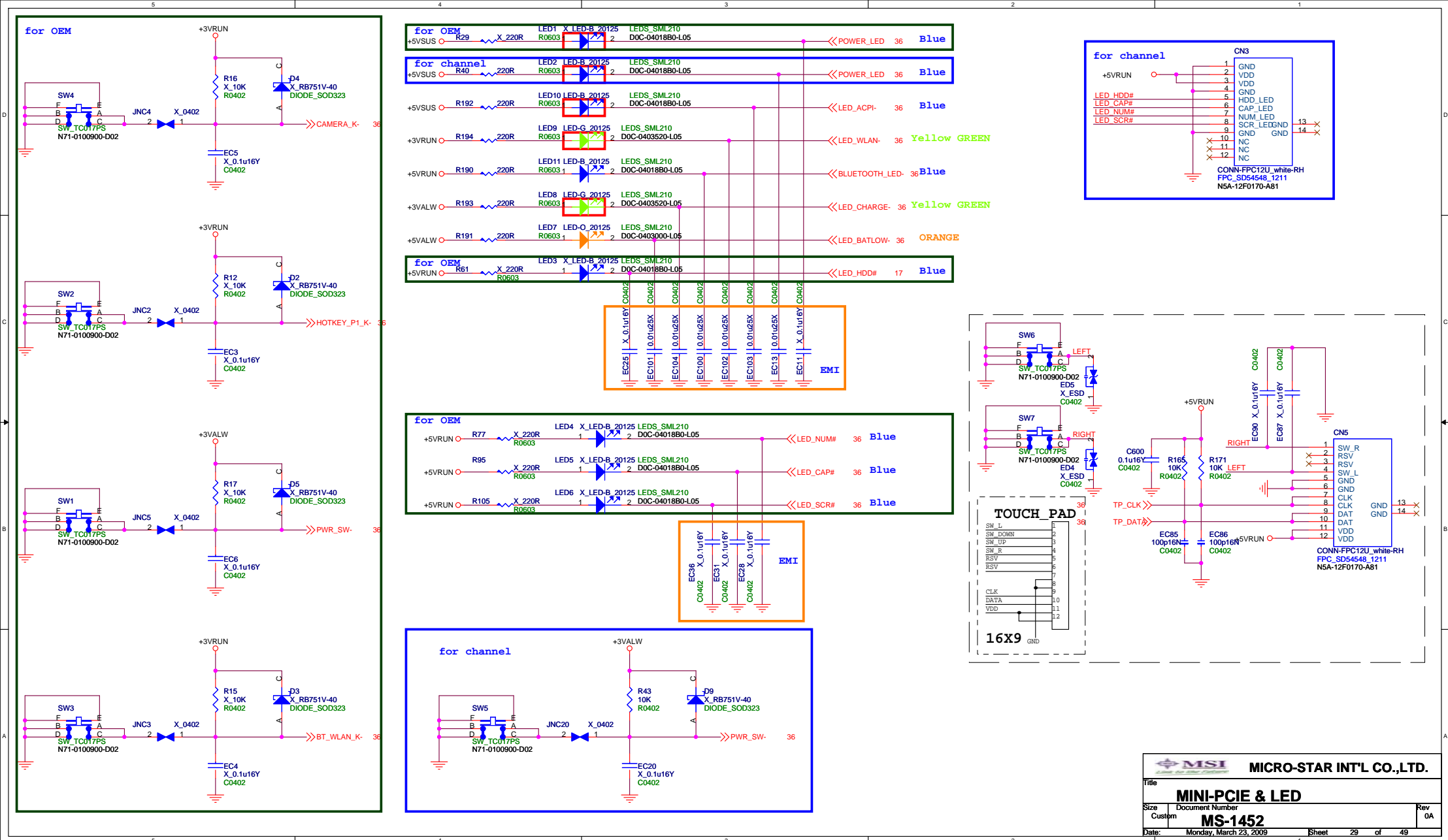
Adobe Acrobat Professional - [PCI_Express_Mini_CEM_10.pdf]

Power Rail	Voltage Tolerance	Primary Power*		Auxiliary Power**
		Peak (max) mA	Normal (max) mA	Normal (max) mA
+3.3V	±9%	1,000	750	
3.3Vaux	±9%	330	250	250 (wake enabled) 5 (not wake enabled)
+1.5V	±5%	500	375	N/A

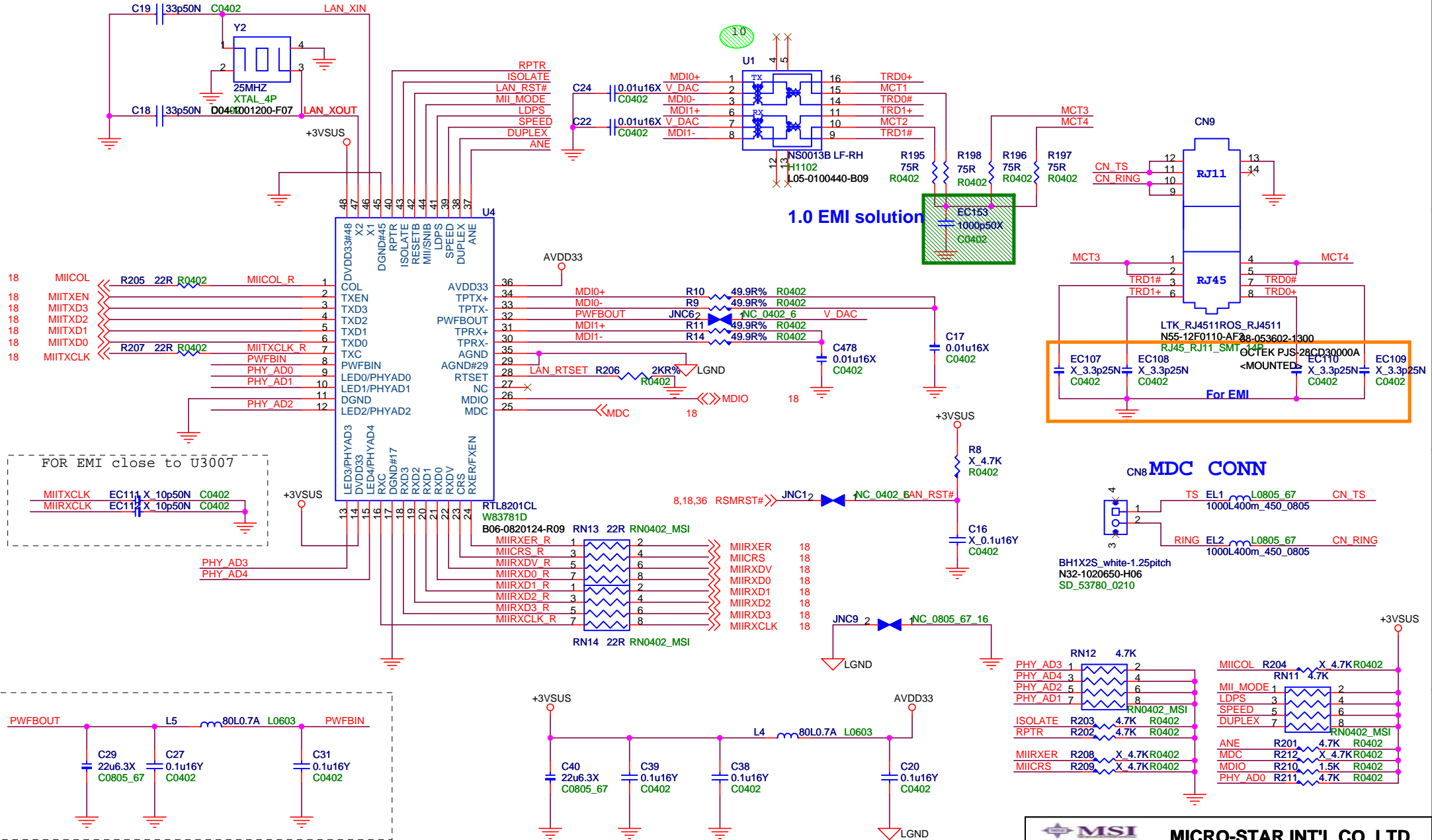


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Title: **NEW CARD & MDC**
 Size: Cuspm
 Document Number: **MS-1452**
 Date: Monday, March 23, 2009 Sheet 28 of 49 Rev 0A



LAN MAGNETICS



please C3088,C3089,L3007 close to PWFBOUT(U3007.32)
and C3090 close to PWFBIN (U3007.8)


MICRO-STAR INT'L CO.,LTD.

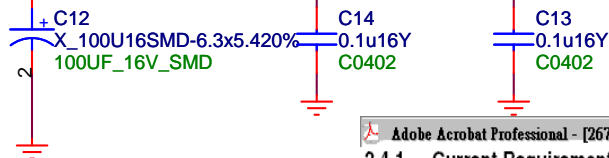
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Size Custom	Document Number MS-1452	Rev 0A
Date: Monday, March 23, 2009	Sheet 30	of 49

2.5" HD DRIVE

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17 SATA_TXN0_C
17 SATA_RXN0_C
17 SATA_RXP0_C

Near CN4

+5V_{RUN}

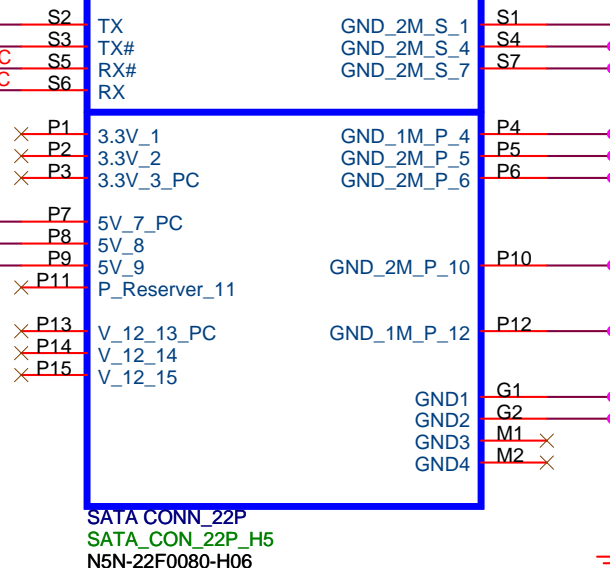


Adobe Acrobat Professional - [2679-701112-A00_SATA_HD.pdf]

2.4.1 Current Requirements and Power Dissipation

Operating Mode	RMS Current ¹	Power, Average ¹
	5 VDC	
Spinup (max)	1000 mA	5.0W
Spinup	700 mA	3.5W
Read/Write	500 mA	2.5W
Seek	500 mA	2.5W

H.D.D.



http://172.16.0.182-84/temporal_approval/S7D-2280001-SI4/BC-5500S-01_rev_003.pdf

10.1.2 CURRENT (Max or Typical)

22 / 27

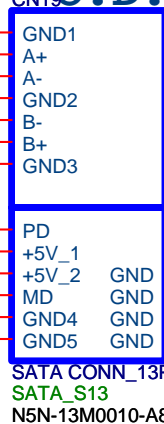
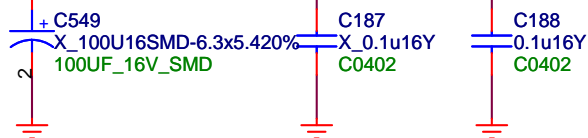
Sleep	110mA max
Standby	110mA max
Continuous Read (CD)	950mA typical
Continuous Read (DVD)	1150mA typical
Continuous Read (BD)	1250mA typical
Continuous Write (CD)	1100mA typical
Continuous Write (DVD)	1200mA typical
Maximum	1700mA max

O.D.D.

17 SATA_TXP1_C
17 SATA_TXN1_C
17 SATA_RXN1_C
17 SATA_RXP1_C

Near CN5

+5V_{RUN}



MICRO-STAR INT'L CO.,LTD.

Title

SATA HDD/ODD

Size
A

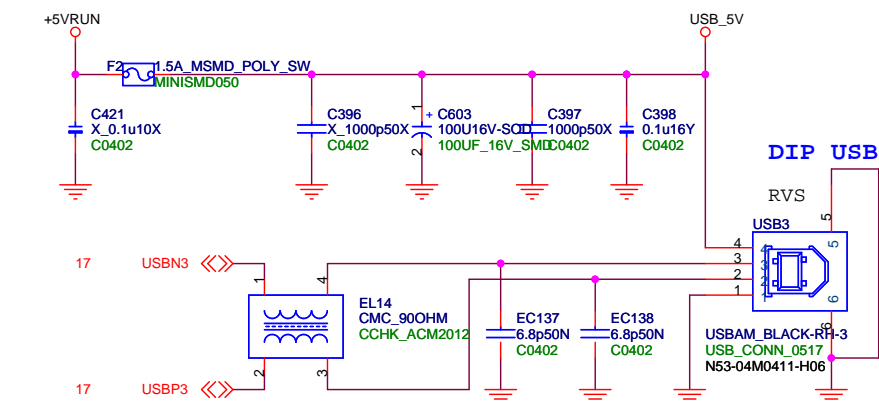
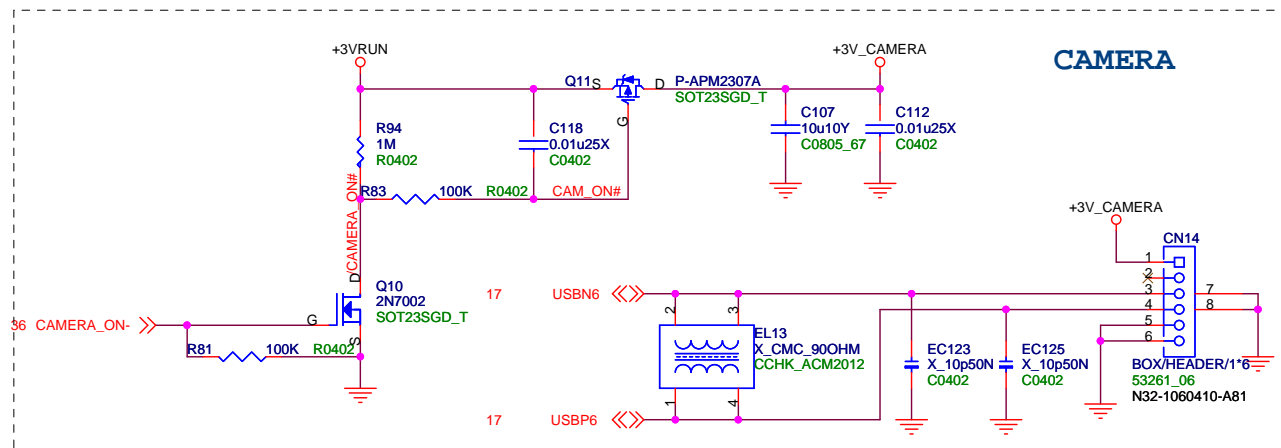
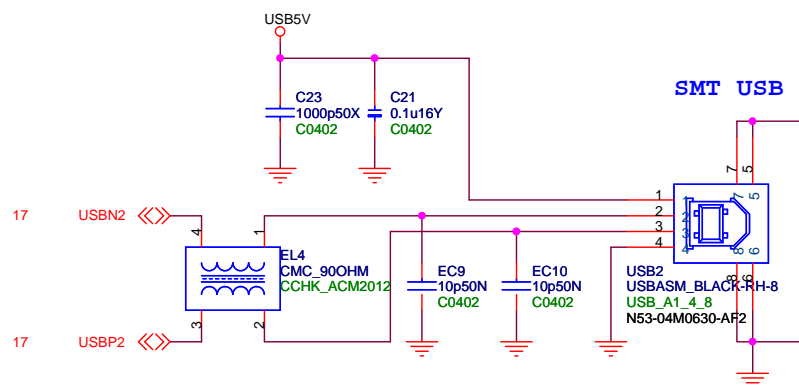
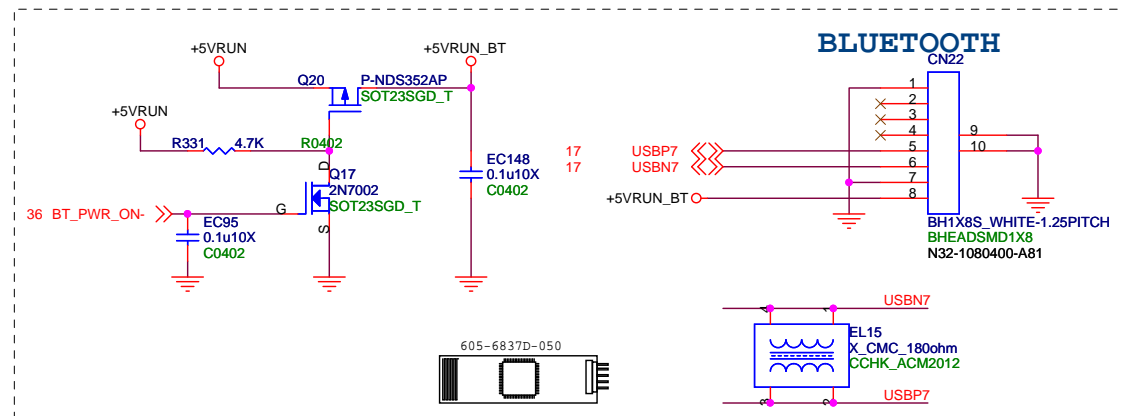
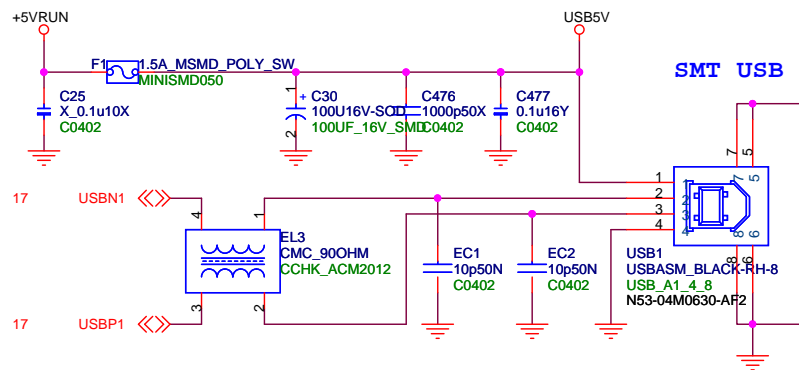
Document Number

MS-1452

Rev
0A

Date: Monday, March 23, 2009

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[ACME-PF13006-1*20Product*20Specification-B_02_Jan30_.pdf]

Module Specification

Function	Description
Module Dimension	8.9(W)x60.0(L)x5.25(H)mm
Power Consumption	Ready: <80mA (USB ready, sensor disabled) Active: <150mA Suspend: <1mA (USB selective suspend mode)
Operating Temperature	0°C ~ 60°C
Storage Temperature	-20°C ~ 80°C

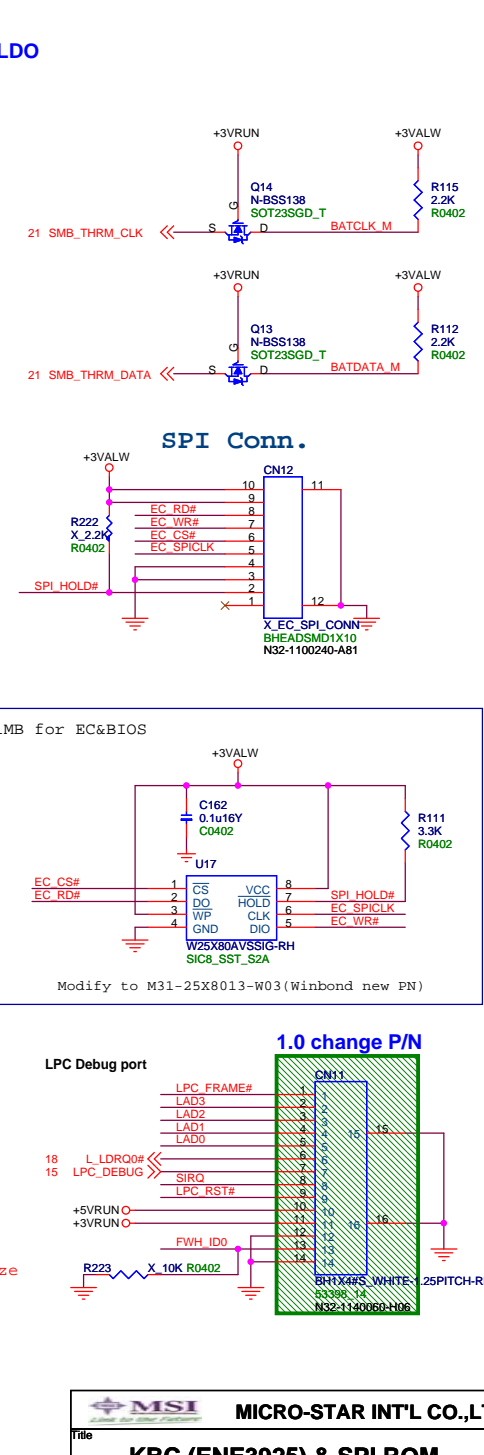
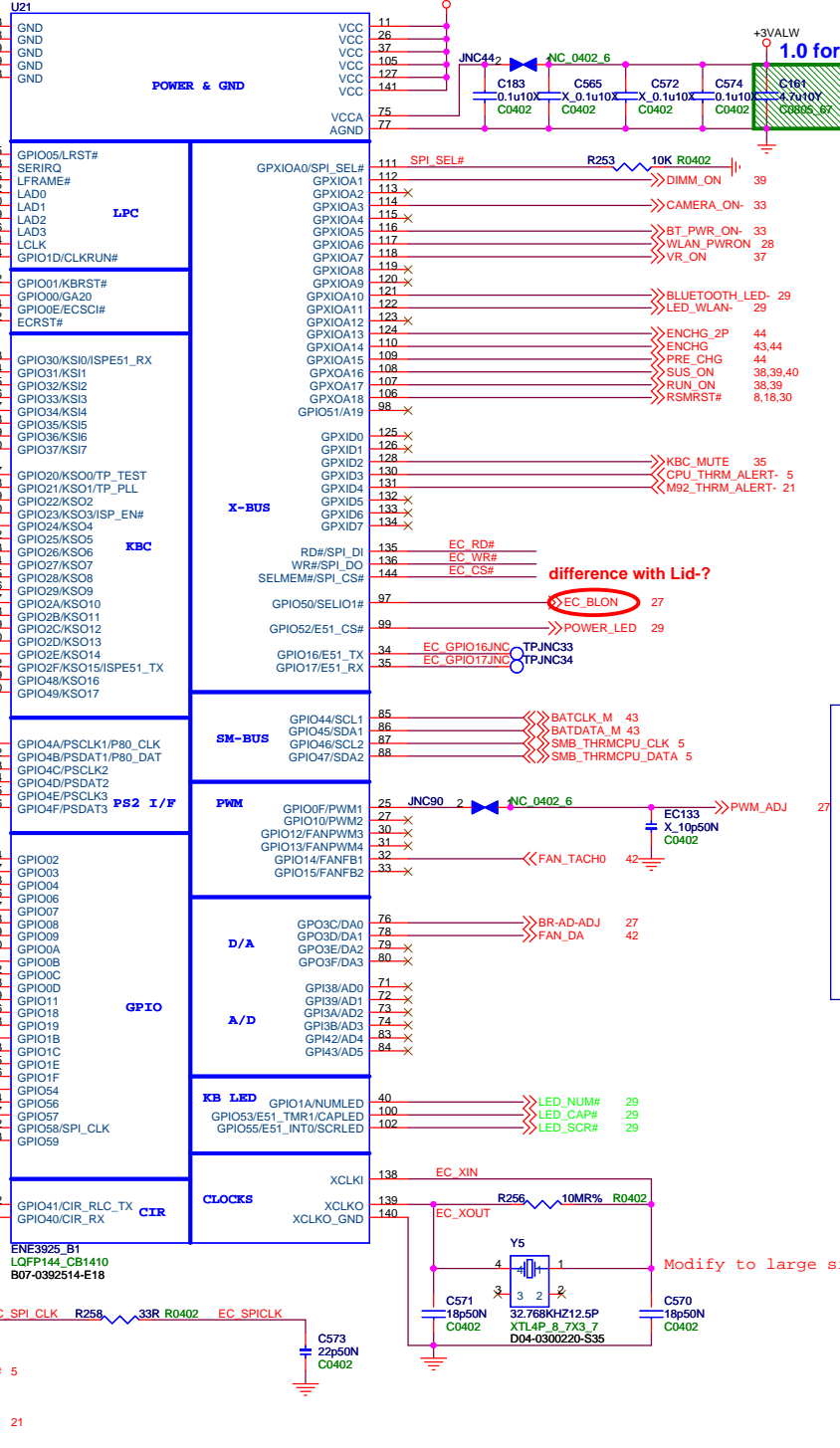
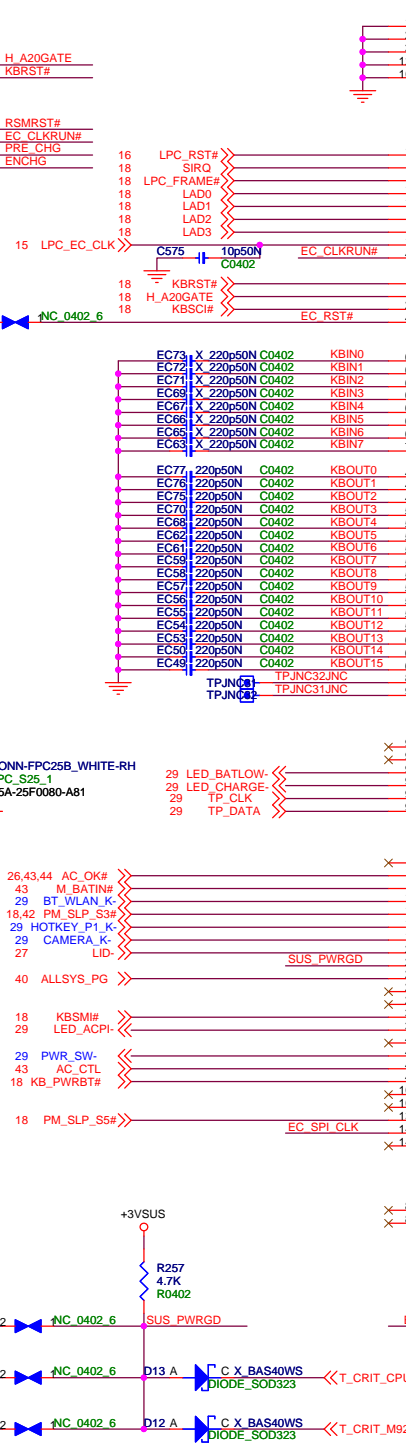
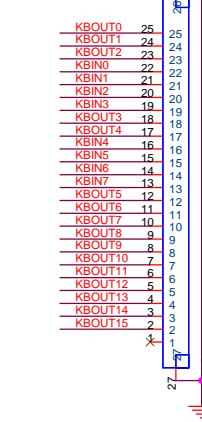
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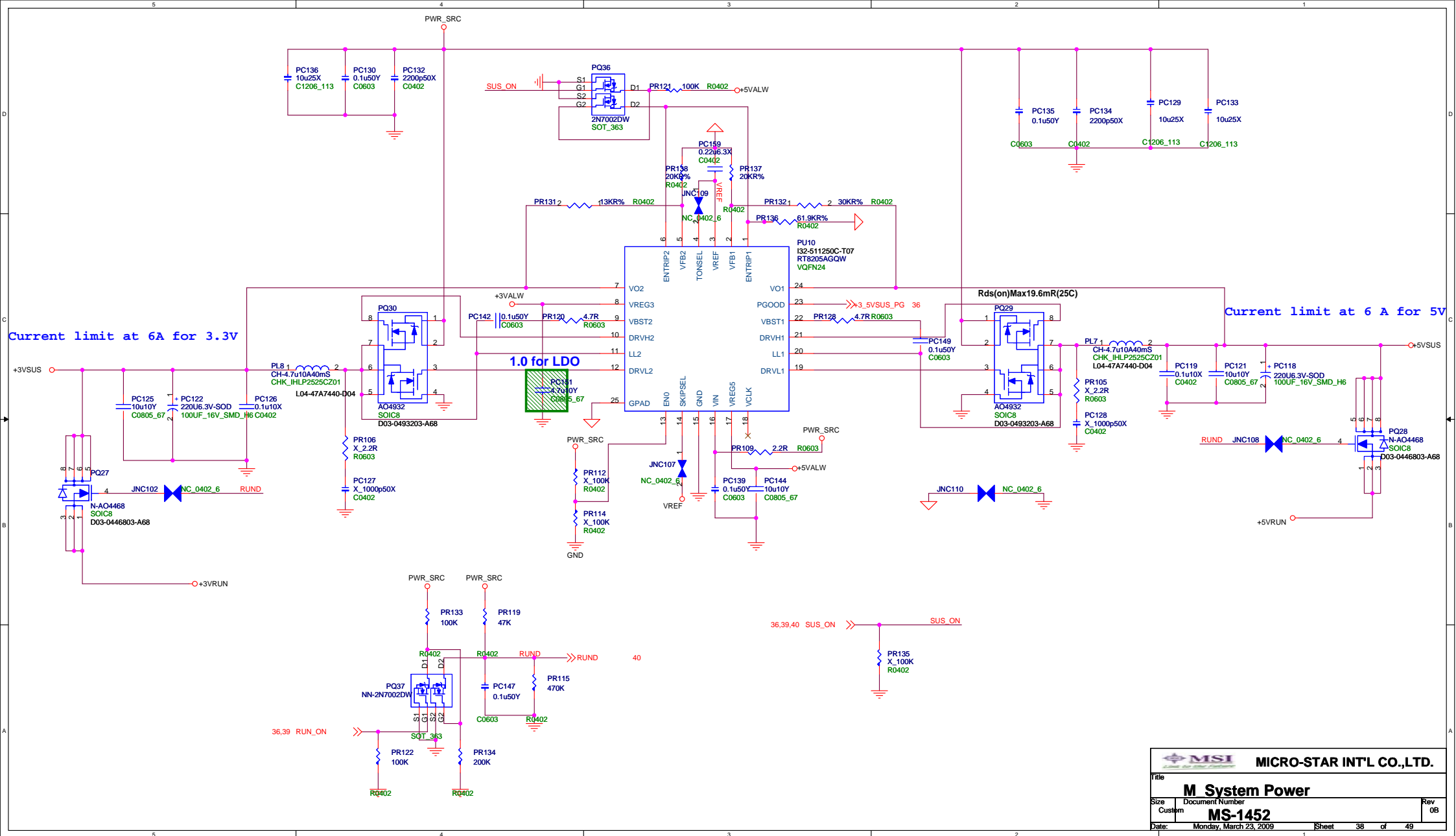
Title **USBx3,BT,CAMERA**

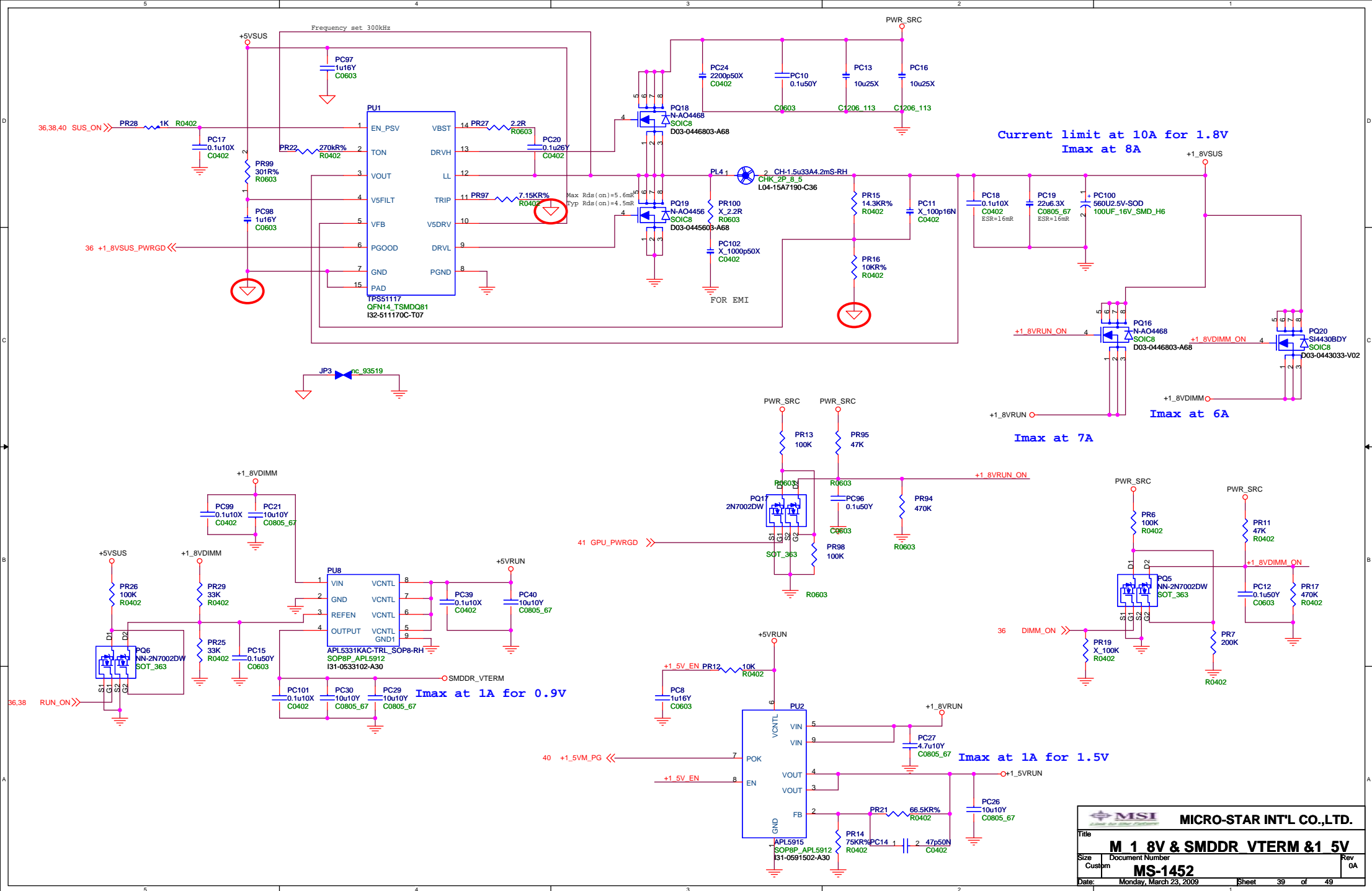
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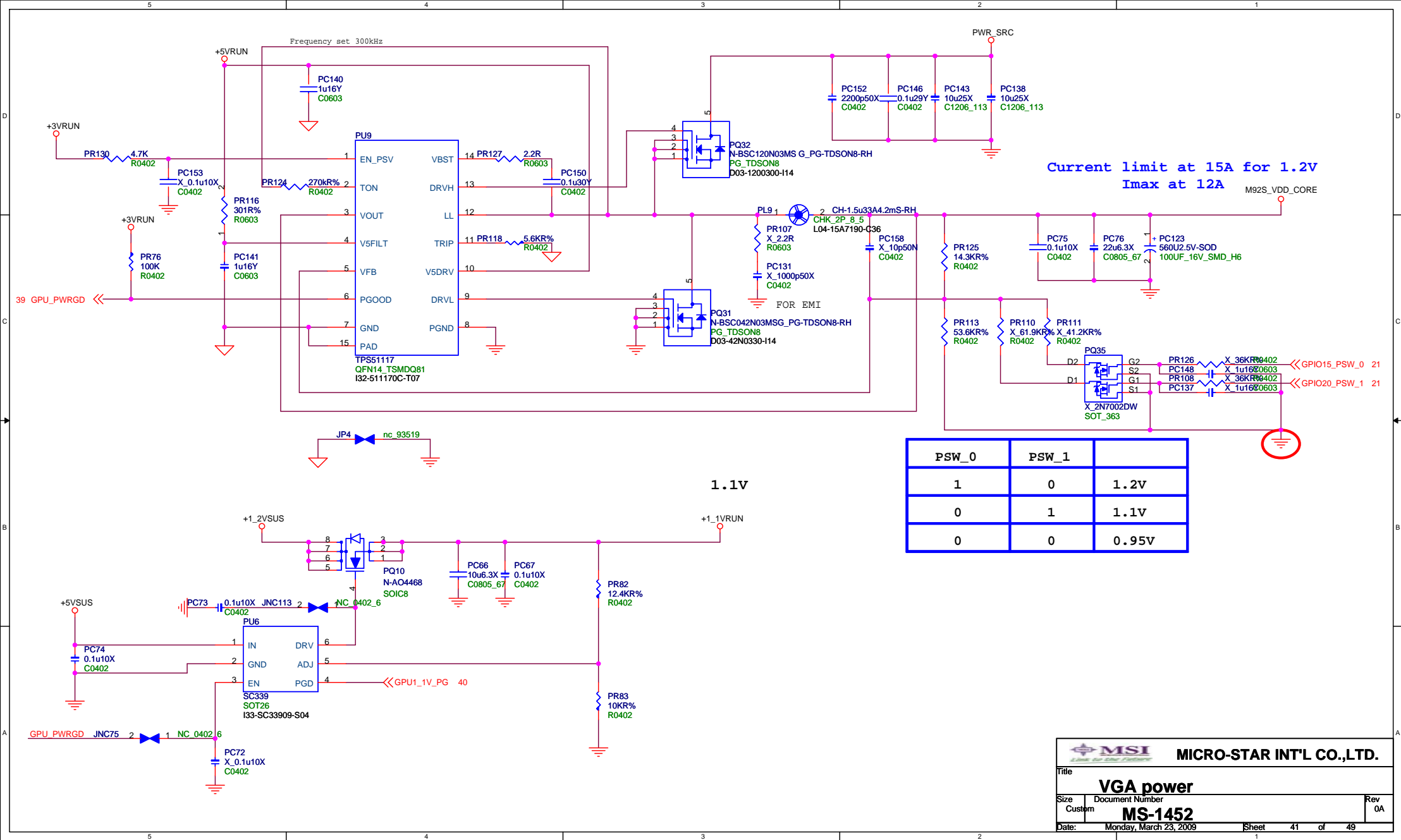
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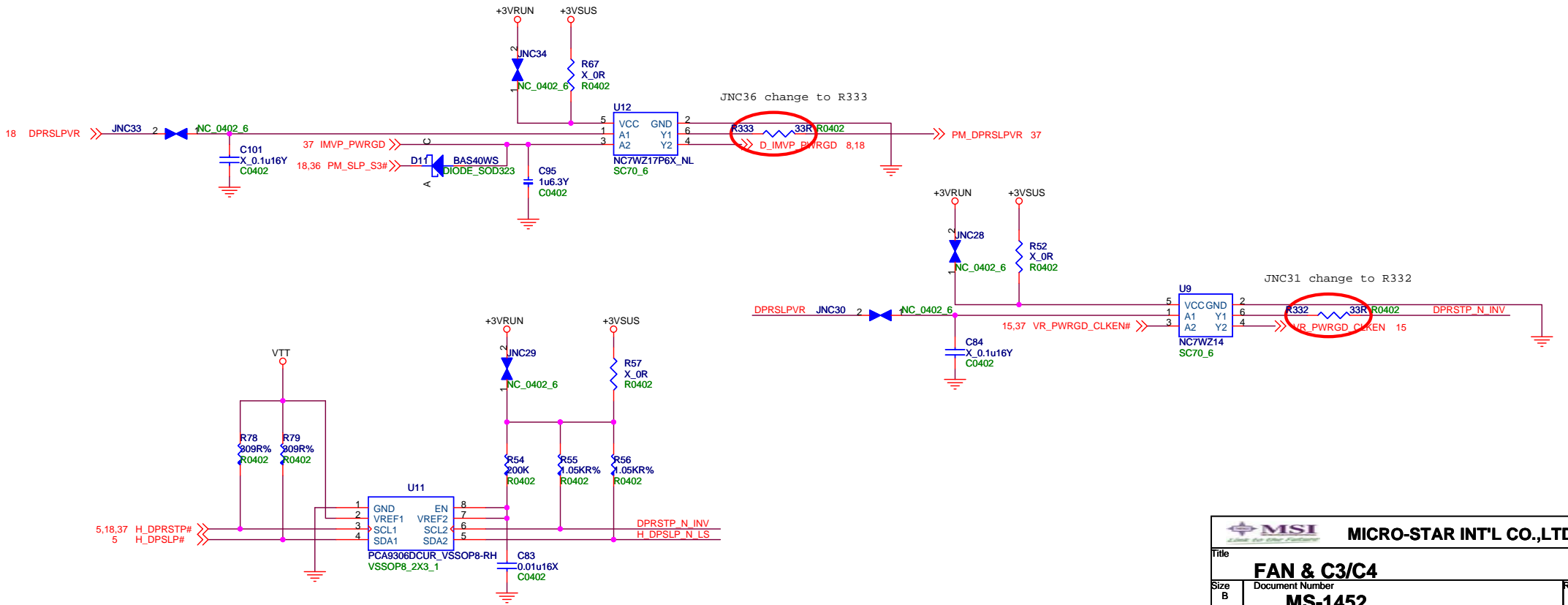
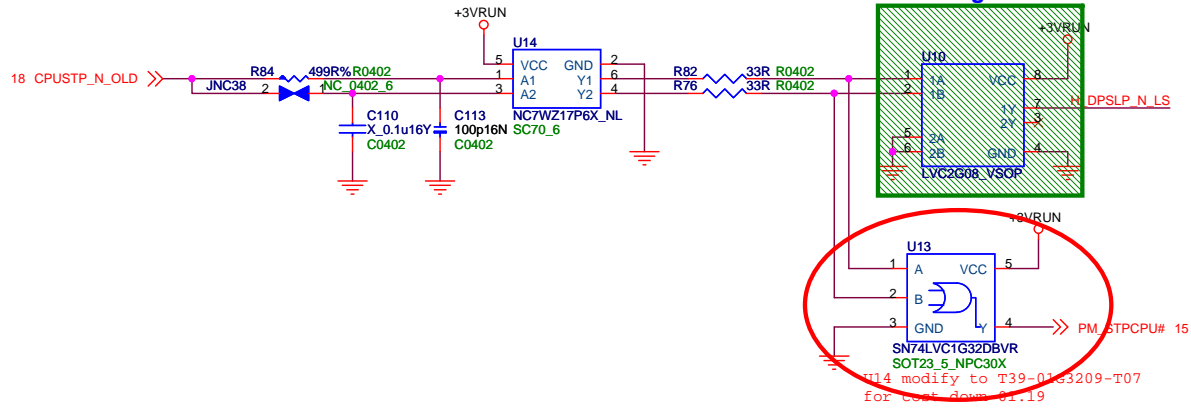
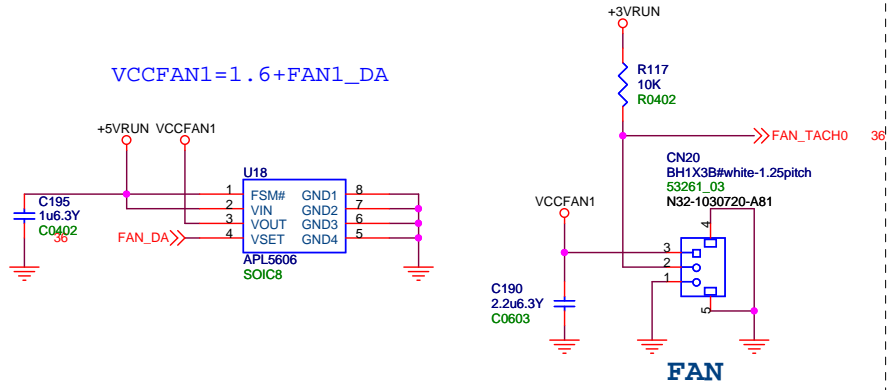


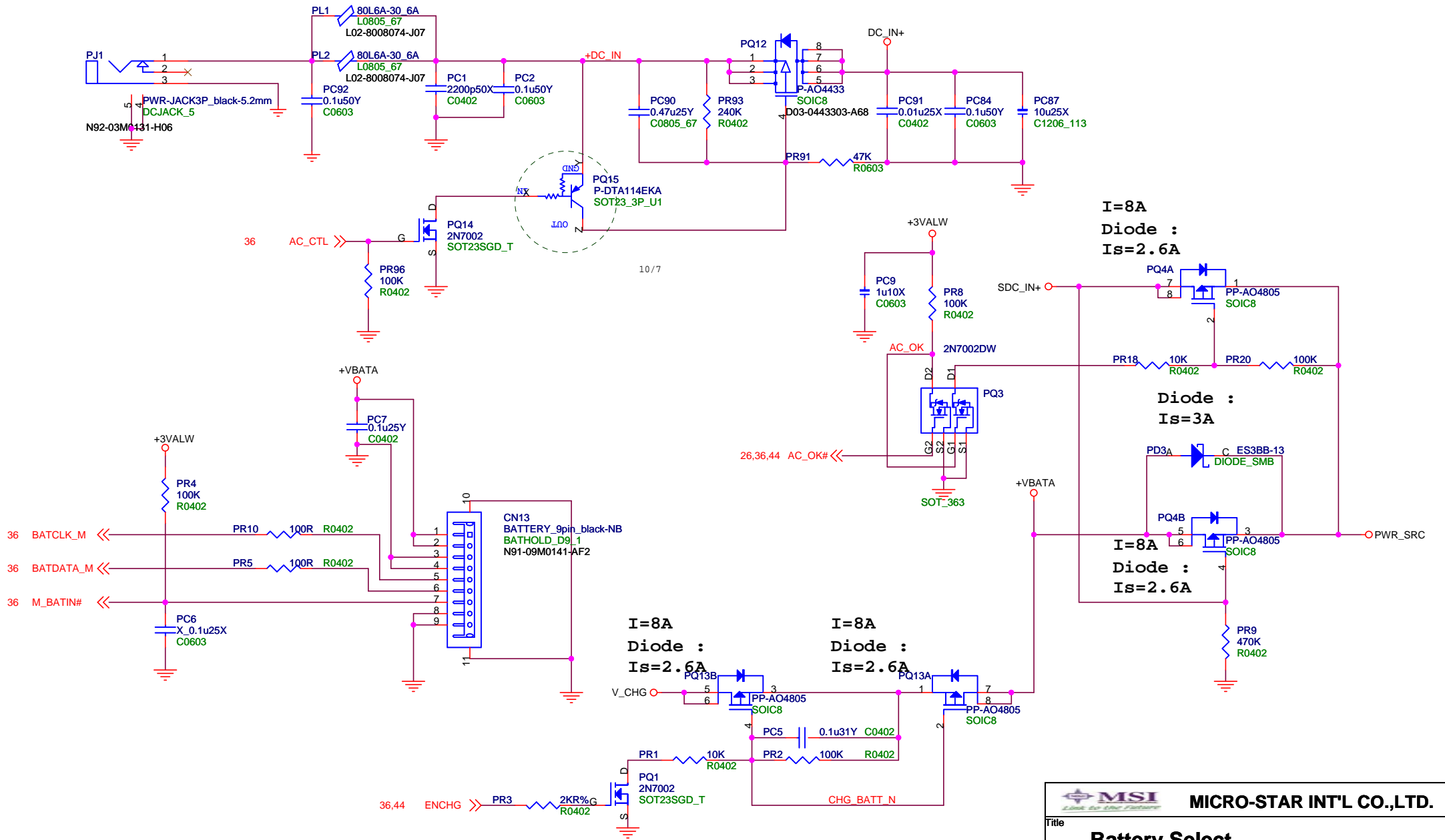





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Title M 1 8V & SMDDR VTERM &1 5V			
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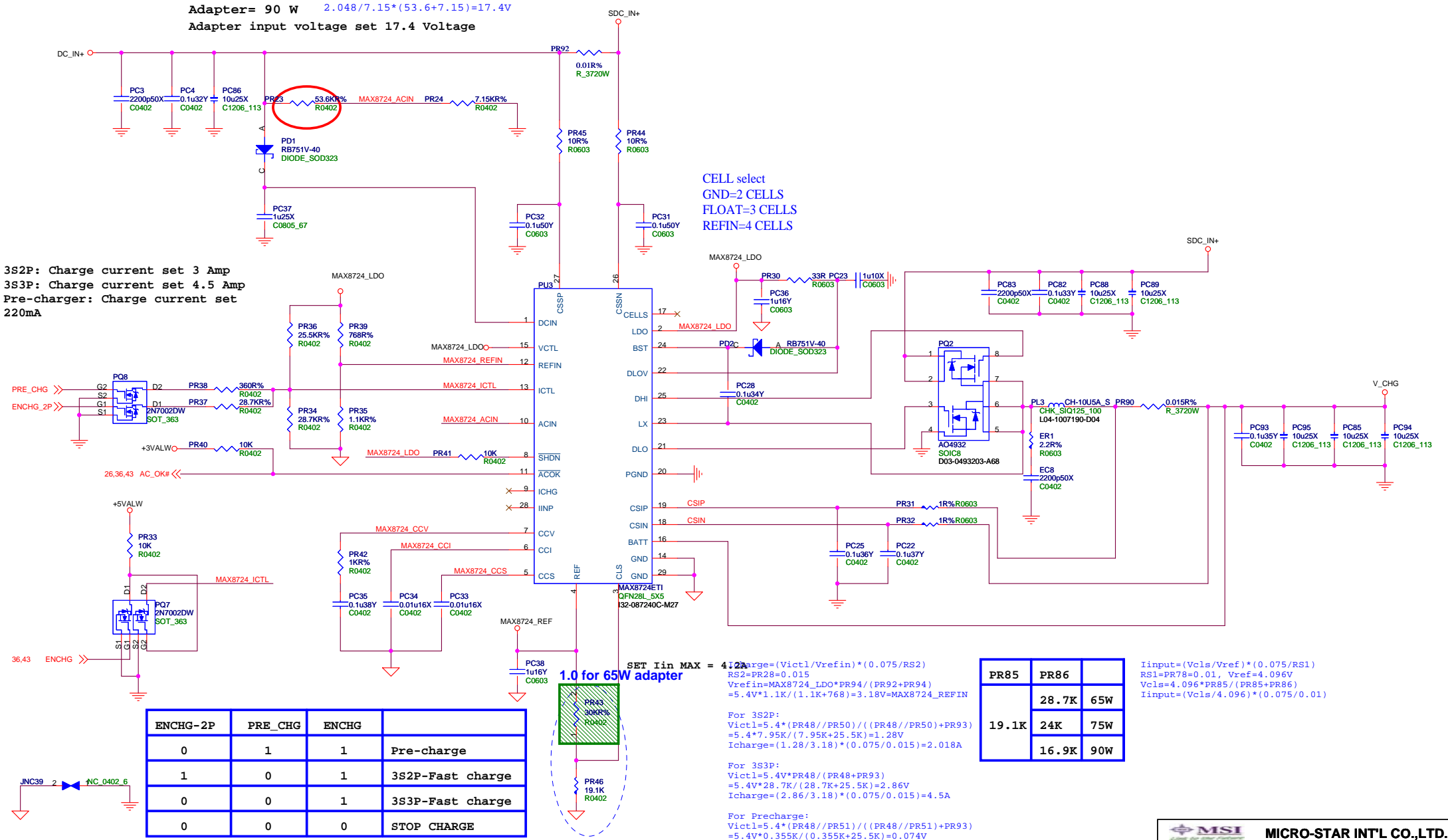


**MICRO-STAR INT'L CO.,LTD.**

Title		
Battery Select		
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Adapter= 90 W $2.048/7.15*(53.6+7.15)=17.4V$
 Adapter input voltage set 17.4 Voltage

3S2P: Charge current set 3 Amp
 3S3P: Charge current set 4.5 Amp
 Pre-charger: Charge current set 220mA



CELL select
 GND=2 CELLS
 FLOAT=3 CELLS
 REFIN=4 CELLS

SET Iin MAX = 4.12A

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

For 3S2P:
 $V_{ict1} = 5.4V * (PR48 / (PR50 + ((PR48 / PR50) + PR93)))$
 $= 5.4V * 7.95K / (7.95K + 25.5K) = 1.28V$
 $I_{charge} = (1.28V / 3.18) * (0.075 / 0.015) = 2.018A$

For 3S3P:
 $V_{ict1} = 5.4V * (PR48 / (PR50 + ((PR48 / PR50) + PR93)))$
 $= 5.4V * 28.7K / (28.7K + 25.5K) = 2.86V$
 $I_{charge} = (2.86V / 3.18) * (0.075 / 0.015) = 4.5A$

For Precharge:
 $V_{ict1} = 5.4V * (PR48 / (PR51 + ((PR48 / PR51) + PR93)))$
 $= 5.4V * 0.355K / (0.355K + 25.5K) = 0.074V$
 $I_{charge} = (0.074mV / 3.18) * (0.075 / 0.015) = 116mA$

PR85	PR86	
19.1K	28.7K	65W
	24K	75W
	16.9K	90W

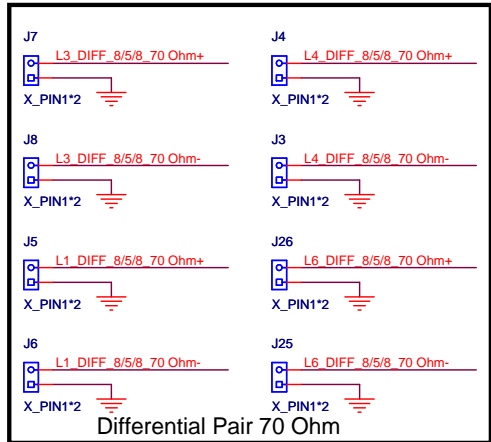
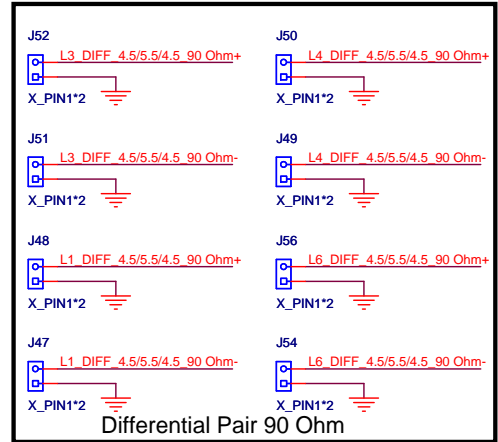
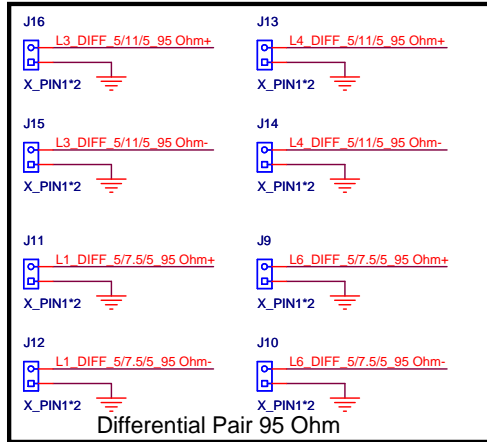
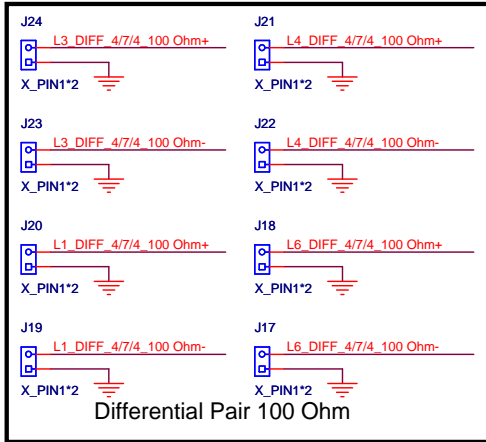
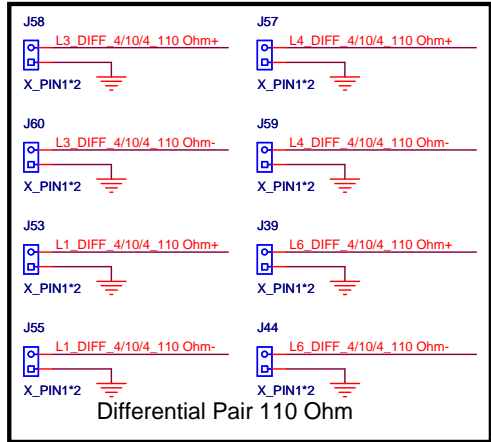
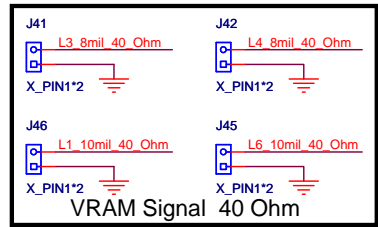
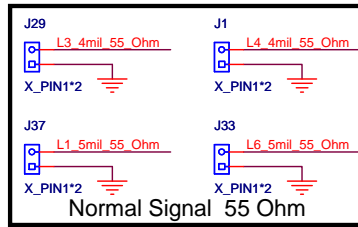
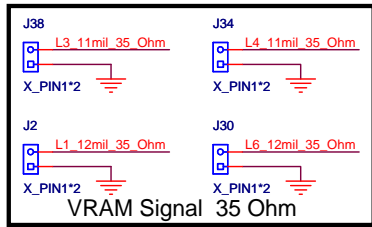
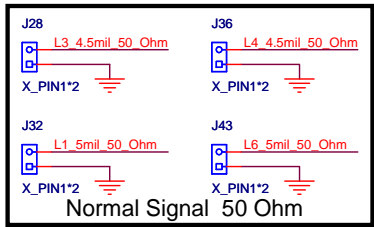
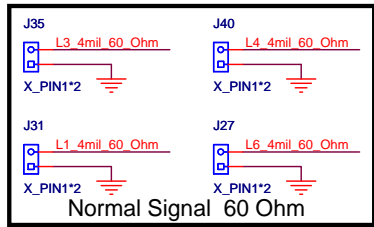
$I_{input} = (V_{cls} / V_{ref}) * (0.075 / RS1)$
 $RS1 = PR78 = 0.01, V_{ref} = 4.096V$
 $V_{cls} = 4.096 * PR85 / (PR85 + PR86)$
 $I_{input} = (V_{cls} / 4.096) * (0.075 / 0.01)$

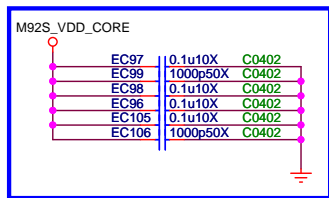
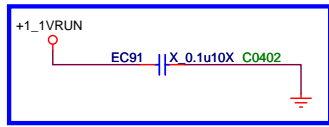
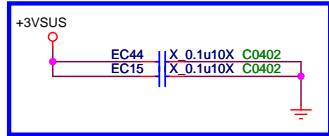
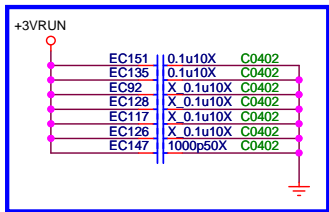
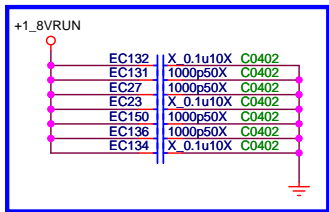
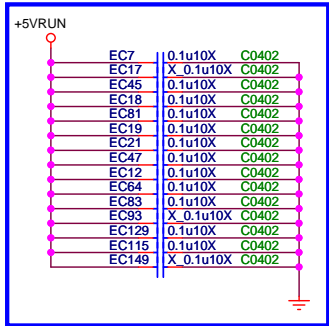
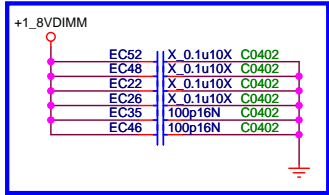
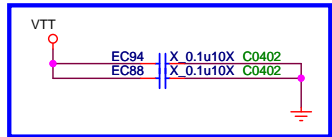
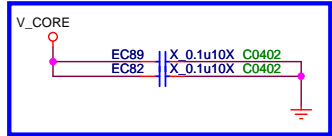
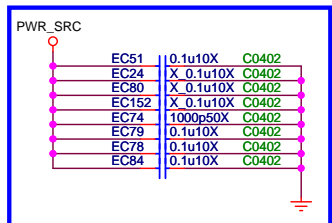
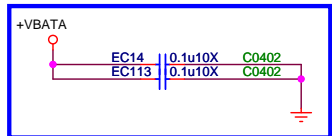
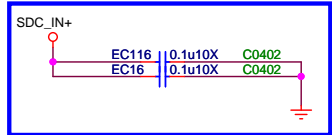
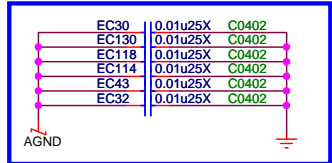
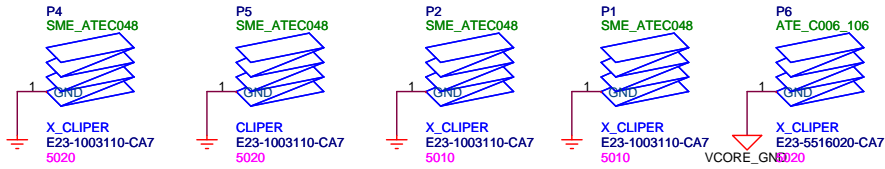
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CHARGER

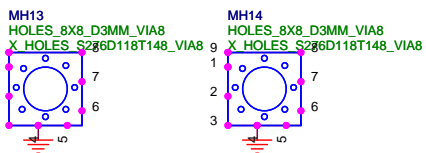
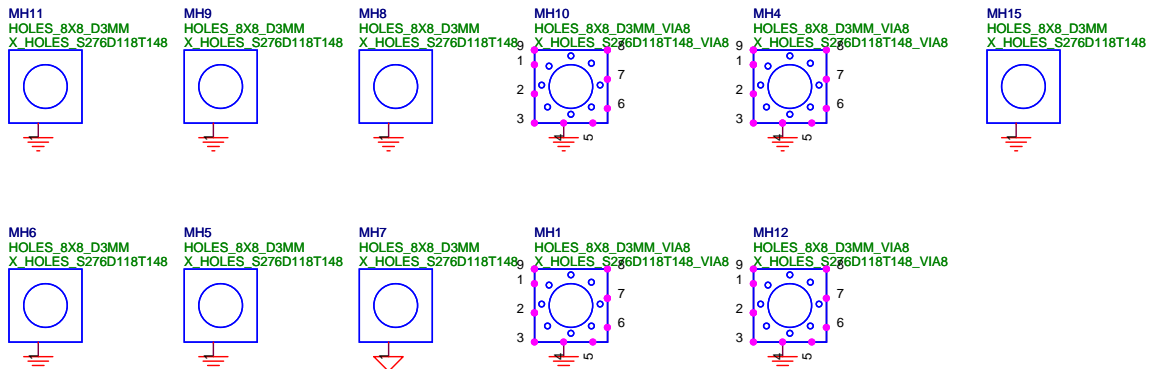
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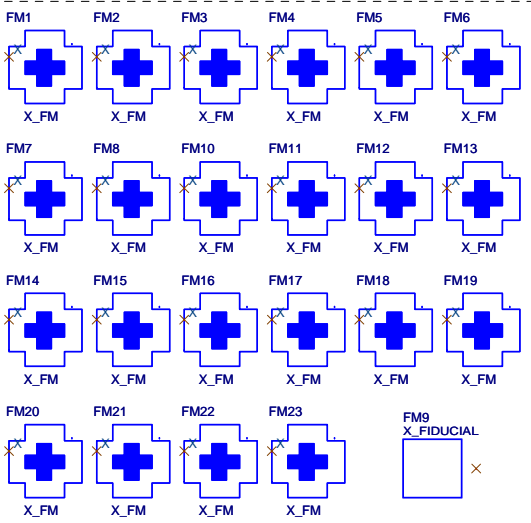
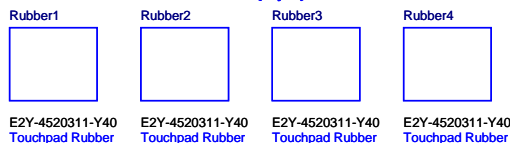




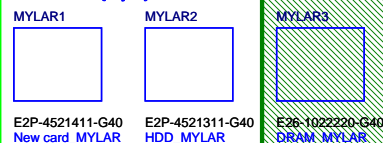
C-case & D-case



60階

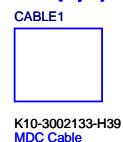


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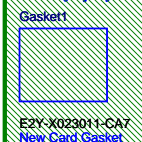
1.0 Add part

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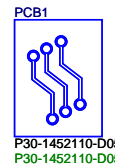


1.0 Add part

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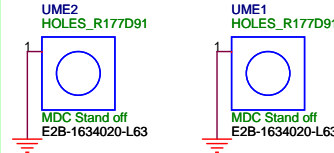


5010階

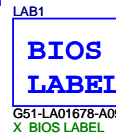
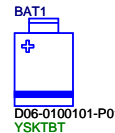


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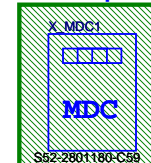
MDC Stand off



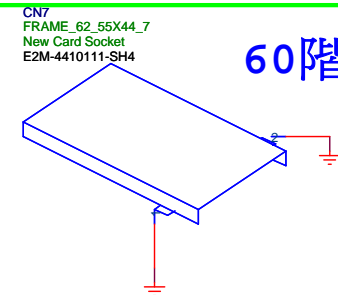
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1.0 DNI part

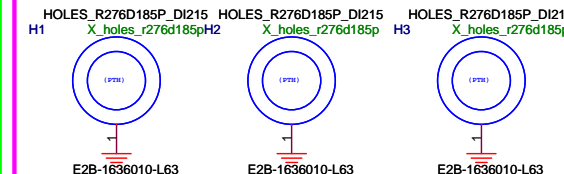


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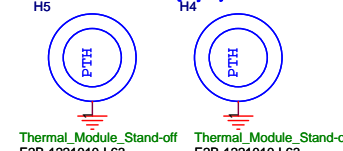
ExpressCard

CPU

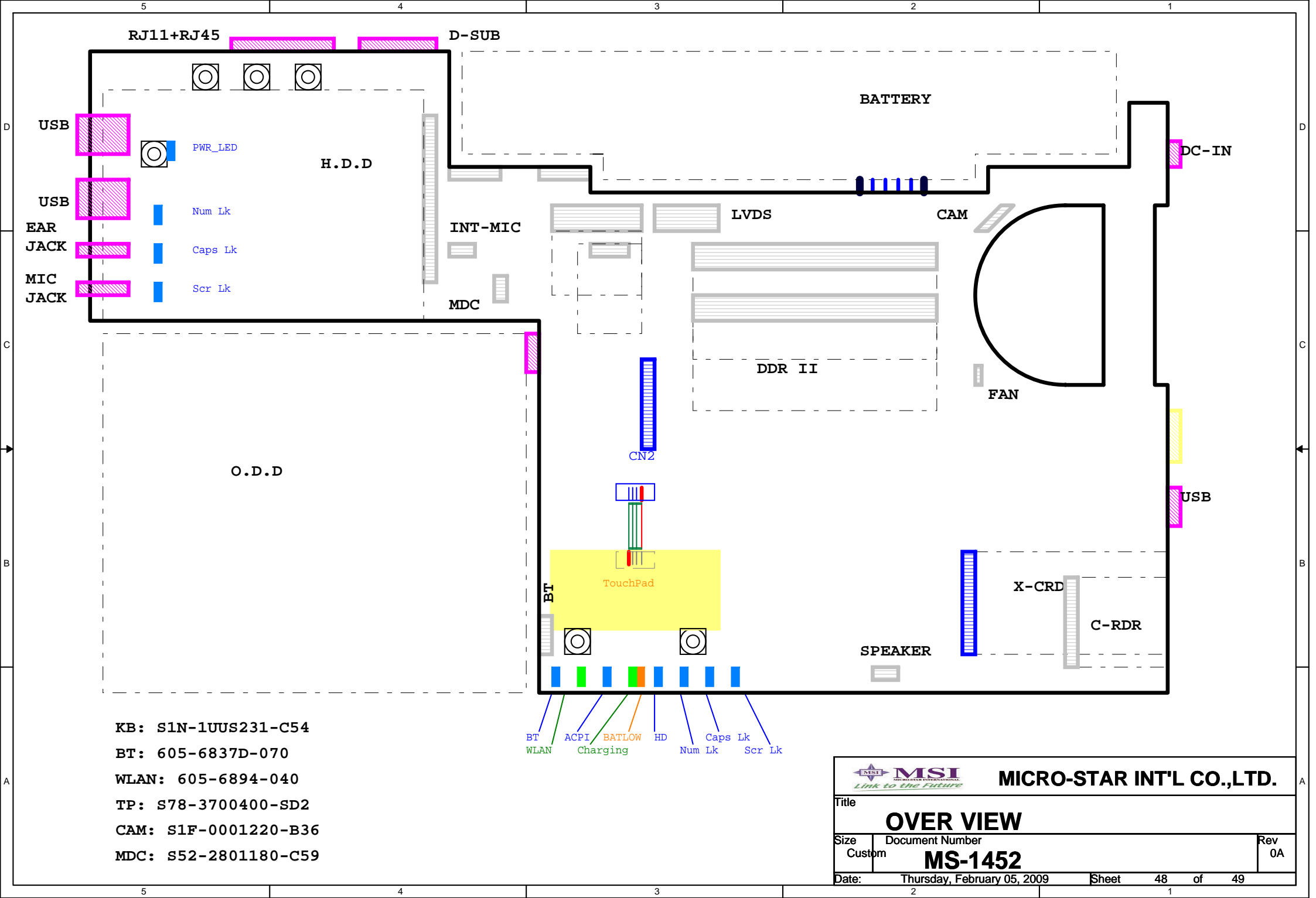


GPU


5020階



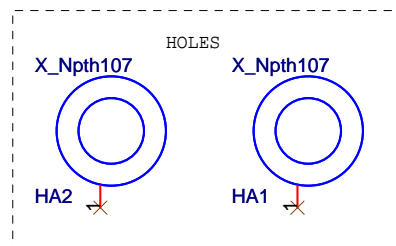
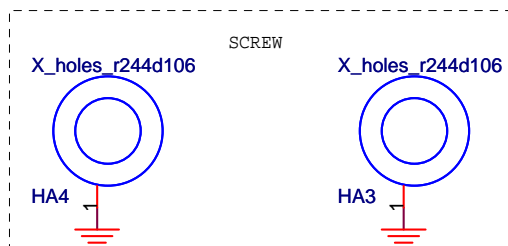
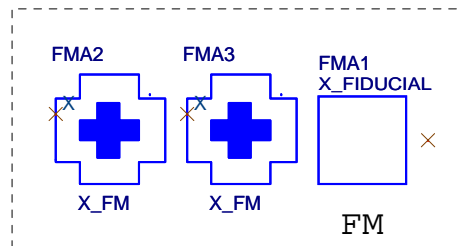
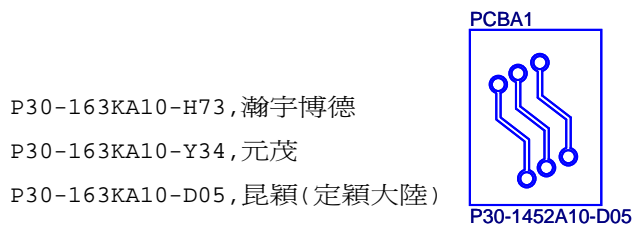
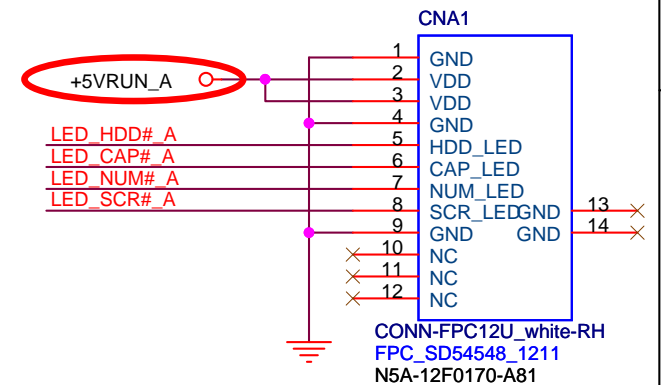
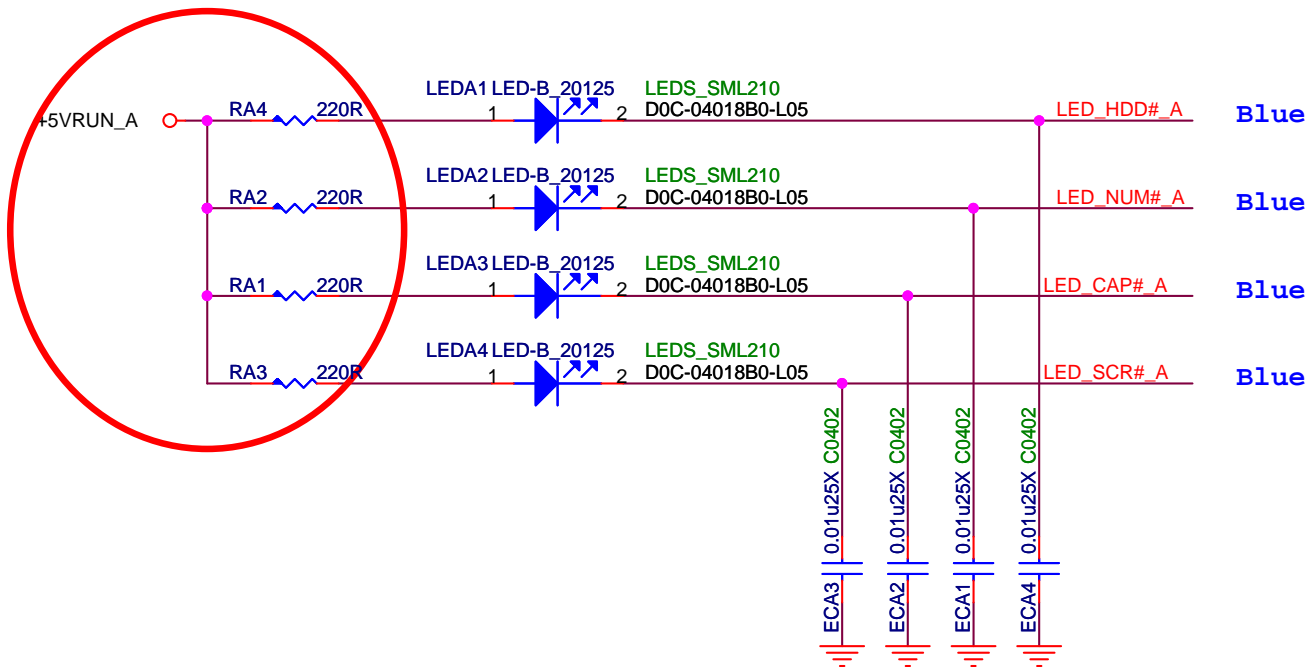
Thermal_Module_Stand-off 螺絲孔




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BT: 605-6837D-070
WLAN: 605-6894-040
TP: S78-3700400-SD2
CAM: S1F-0001220-B36
MDC: S52-2801180-C59

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OVER VIEW	
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for CHANNEL



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LED BOARD		
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